# S71GL512NB0/S71GL256NB0/ S71GL128NB0

## Stacked Multi-chip Product (MCP) 512/256/128 Megabit (32/16/8 M x 16-bit) CMOS 3.0 Volt-only MirrorBit™ Page-mode Flash Memory with 32 Megabit (2M x 16-bit) pSRAM

**ADVANCE INFORMATION**

## Distinctive Characteristics

### MCP Features

- **Power supply voltage of 2.7 to 3.1V**

### High Performance

- **90 ns access time (S71GL128N, S71GL256N)**
- **100 ns access time (S71GL512N)**
- **25 ns page read times**
- **Packages:**
  - 9.0 x 12.0 mm x 1.2 mm FBGA (TLD084) (S71GL512N)
  - 8.0 x 11.6 mm x 1.2 mm FBGA (TLA084) (S71GL128N, S71GL256N)
- **Operating Temperature**
  - -25°C to +85°C (Wireless)
  - -40°C to +85°C (Industrial)

## General Description

The S71GL Series is a product line of stacked Multi-chip Product (MCP) packages and consists of

- One Flash memory die
- one pSRAM

The products covered by this document are listed in the table below. For details about their specifications, please refer to the individual constituent datasheets for further details.

| | | Flash Memory Density | | |
|---|---|---|---|---|
| | | 512 Mb | 256 Mb | 128 Mb |
| pSRAM Density | 128 Mb | | | |
| | 64 Mb | | | |
| | 32 Mb | S71GL512NB0 | S71GL256NB0 | S71GL128NB0 |
| | 16 Mb | | | |

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## S71GL512NB0/S71GL256NB0/S71GLI28NB0



## S29GLxxxN MirrorBit™ Flash Family

## pSRAM Type I



## pSRAM Type 7

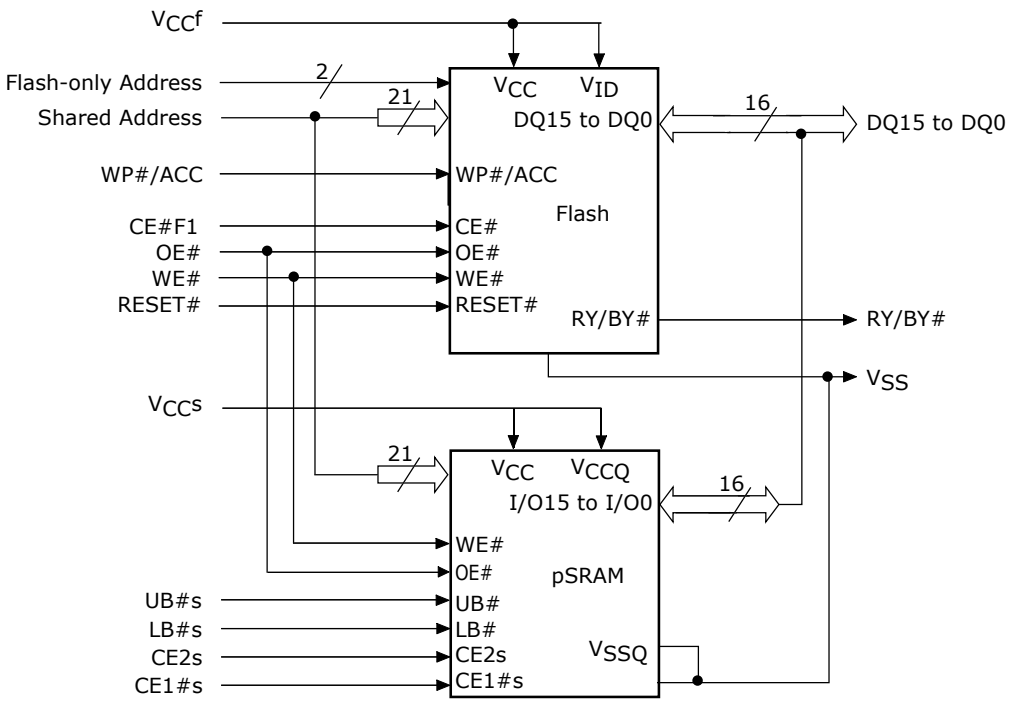
# Product Selector Guide

| S7IGL5I2NB0 | | | |
|---|---|---|---|
| **Access Times at $V_{CC}$ = 2.7 - 3.1 V** | **Flash** | | **pSRAM** |
| Max. Access Time (ns) | 100 | 105 | 65 |
| Max. CE# Access Time (ns) | 100 | 105 | 65 |
| Max. Page Access Time ($t_{PACC}$) | 25 | | 25 |
| Max. OE# Access Time (ns) | 25 | | 25 |

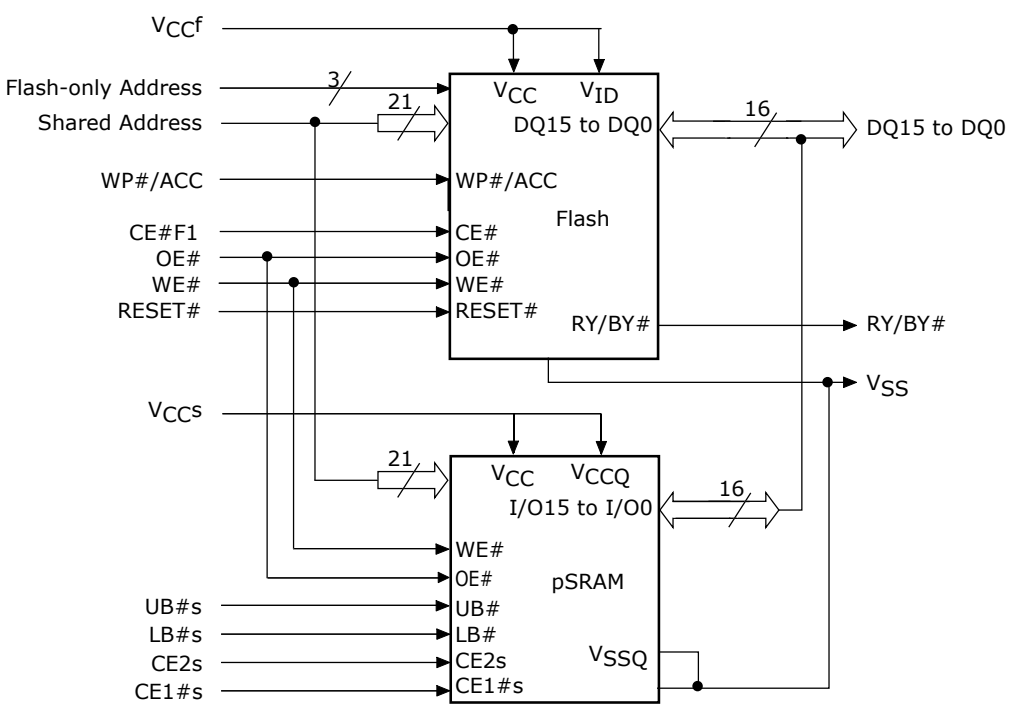
| S7IGL256NB0 | | | |
|---|---|---|---|
| **Access Times at $V_{CC}$ = 2.7 - 3.1 V** | **Flash** | | **pSRAM** |
| Max. Access Time (ns) | 90 | 100 | 65 |
| Max. CE# Access Time (ns) | 90 | 100 | 65 |
| Max. Page Access Time ($t_{PACC}$) | 25 | | 25 |
| Max. OE# Access Time (ns) | 25 | | 25 |

| S7IGLI28NB0 | | | |
|---|---|---|---|
| **Access Times at $V_{CC}$ = 2.7 - 3.1 V** | **Flash** | | **pSRAM** |
| Max. Access Time (ns) | 90 | 100 | 65 |
| Max. CE# Access Time (ns) | 90 | 100 | 65 |
| Max. Page Access Time ($t_{PACC}$) | 25 | | 25 |
| Max. OE# Access Time (ns) | 25 | | 25 |

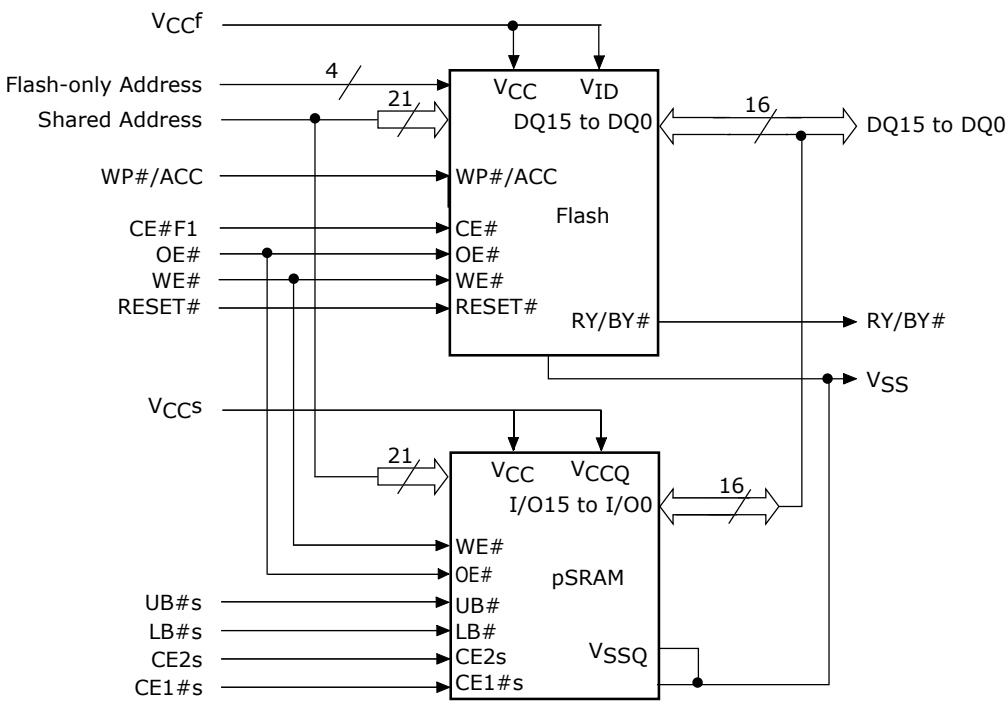
## MCP Block Diagram (128Mb Flash + 32Mb pSRAM)




## MCP Block Diagram (256Mb Flash + 32Mb pSRAM)



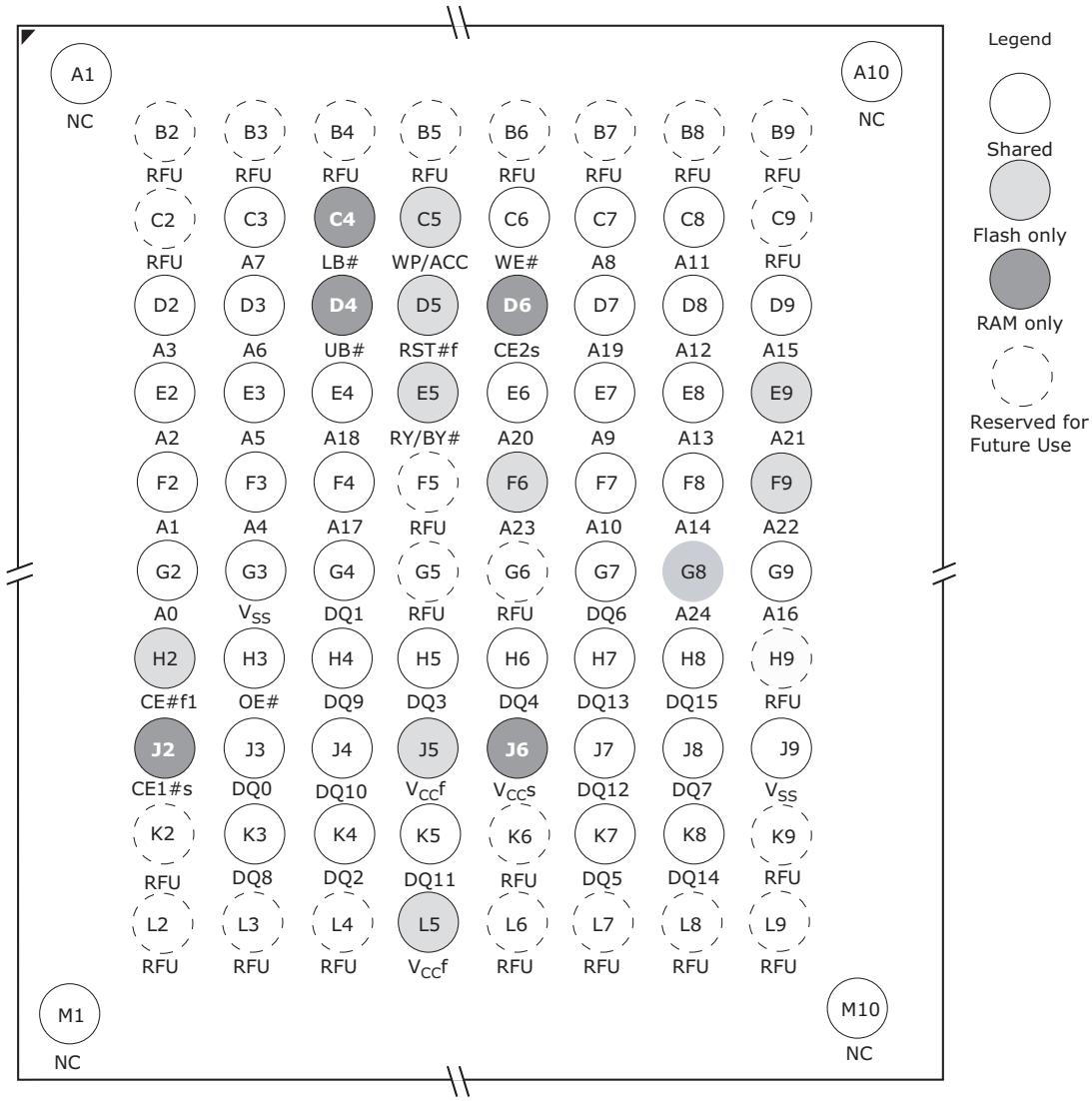
## MCP Block Diagram (512Mb Flash + 32Mb pSRAM)



# Connection Diagrams

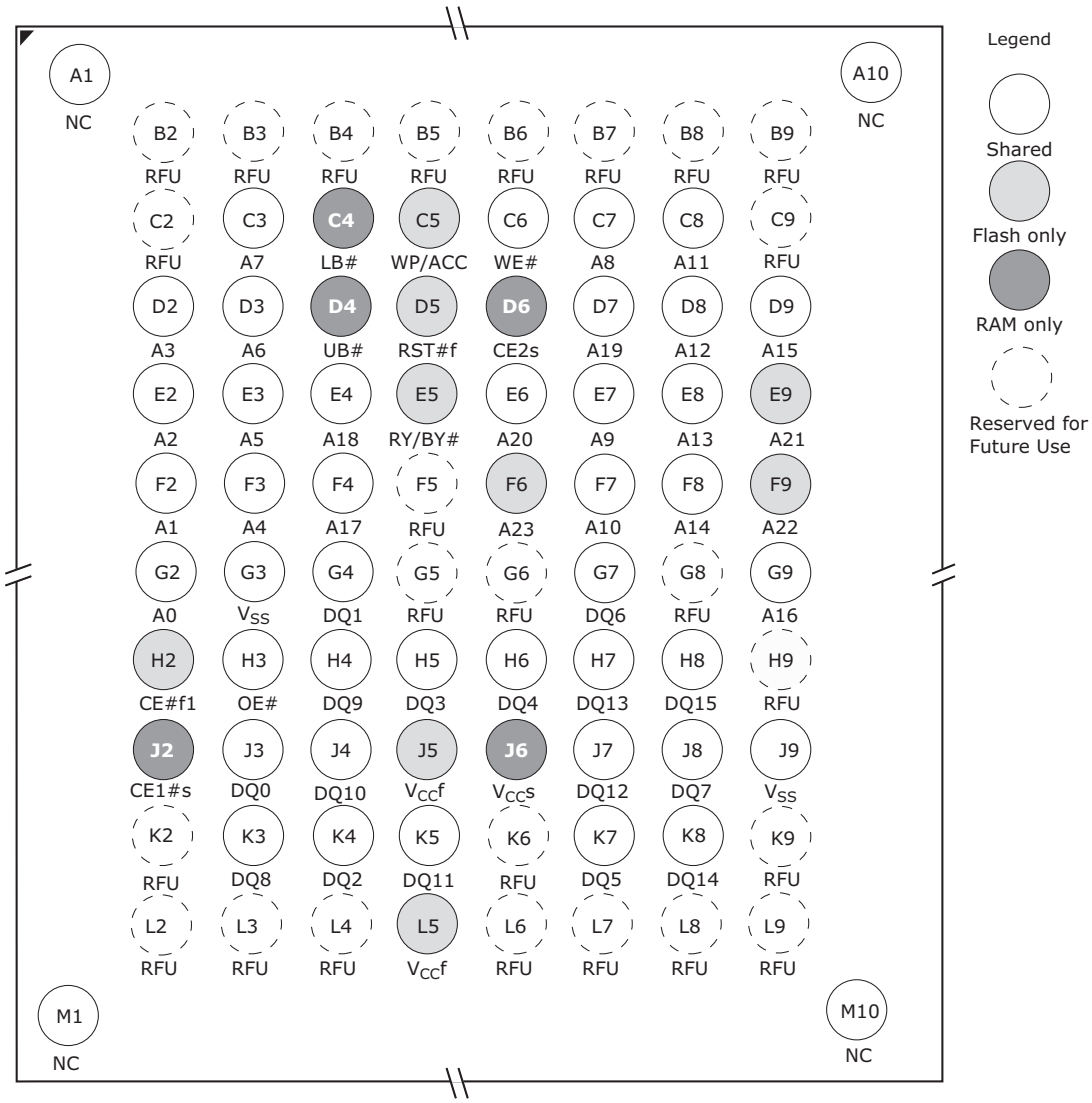
## 512 Mb Flash + 32 Mb pSRAM Pinout

**84-ball Fine-Pitch Ball Grid Array**
**512 Mb Flash + 32 Mb pSRAM**
Pinout
(Top View, Balls Facing Down)



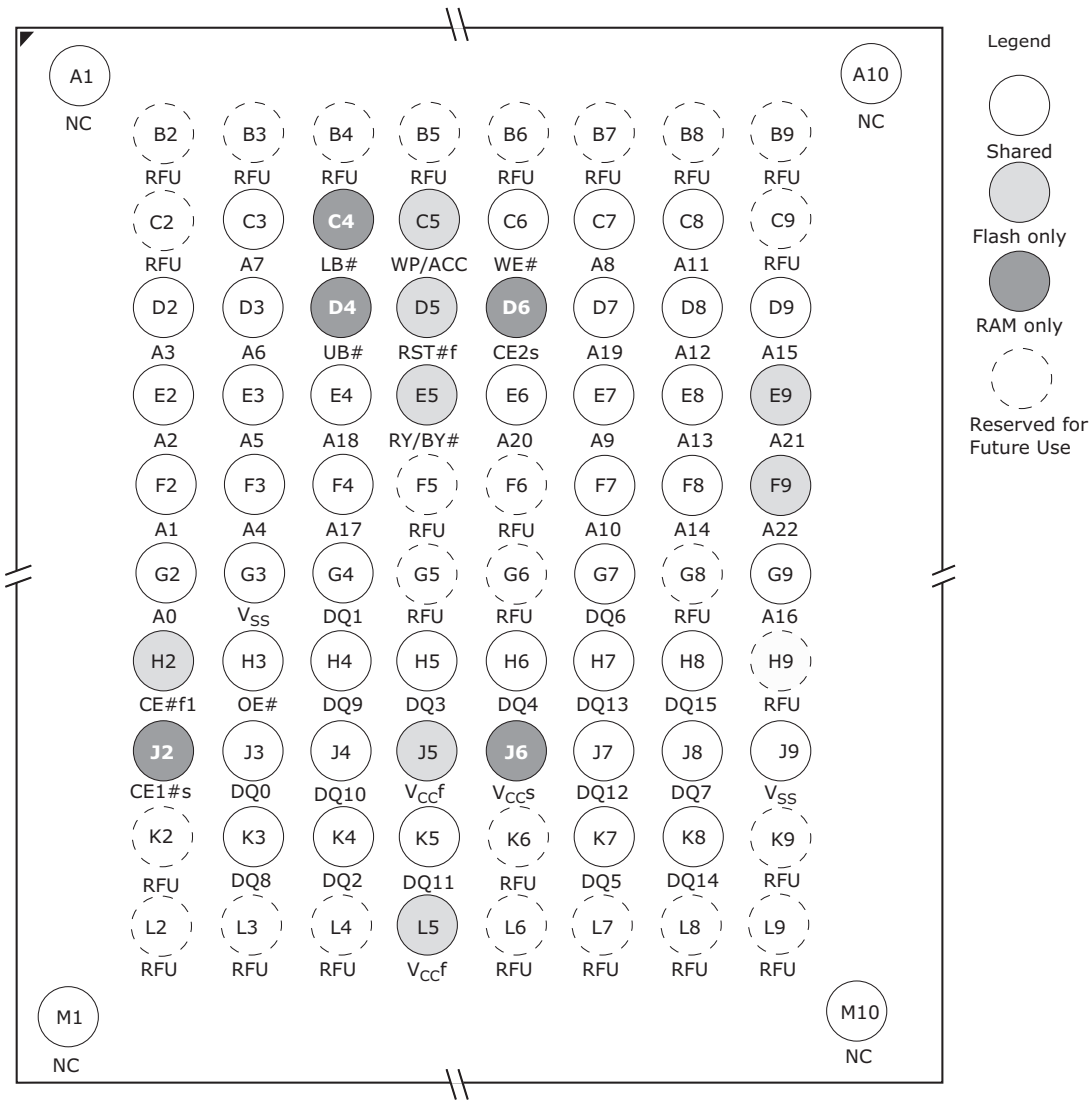
# 256 Mb Flash + 32 Mb pSRAM Pinout

**84-ball Fine-Pitch Ball Grid Array**
**256 Mb Flash + 32 Mb pSRAM**
Pinout
(Top View, Balls Facing Down)



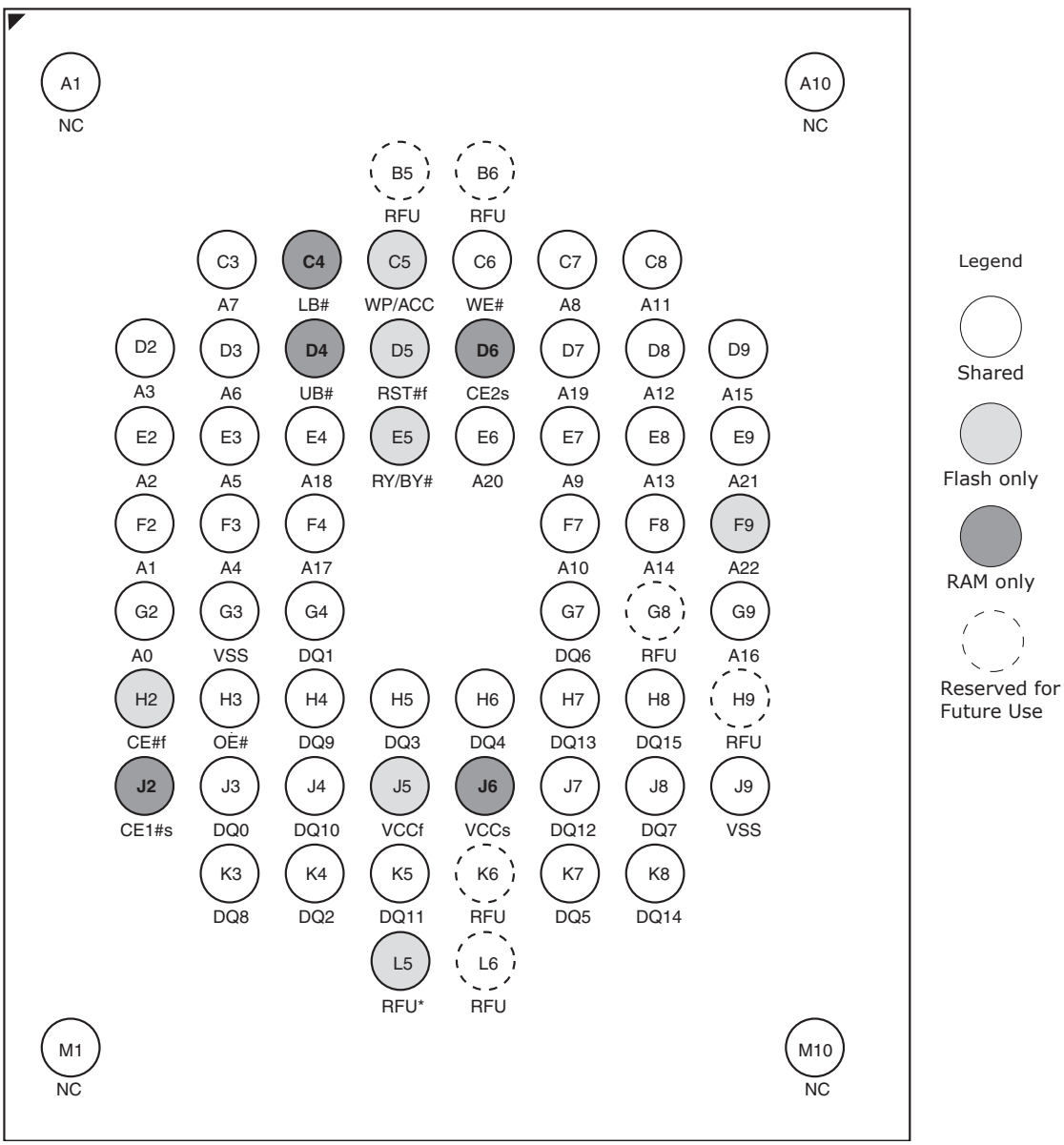
# 128 Mb Flash + 32 Mb pSRAM Pinout

**84-ball Fine-Pitch Ball Grid Array**
**128 Mb Flash + 32 Mb pSRAM**
Pinout
(Top View, Balls Facing Down)



# 128 Mb Flash + 32 Mb pSRAM Pinout (S71GL128NB0 Only)

**64-ball Fine-Pitch Ball Grid Array**
(Top View, Balls Facing Down)

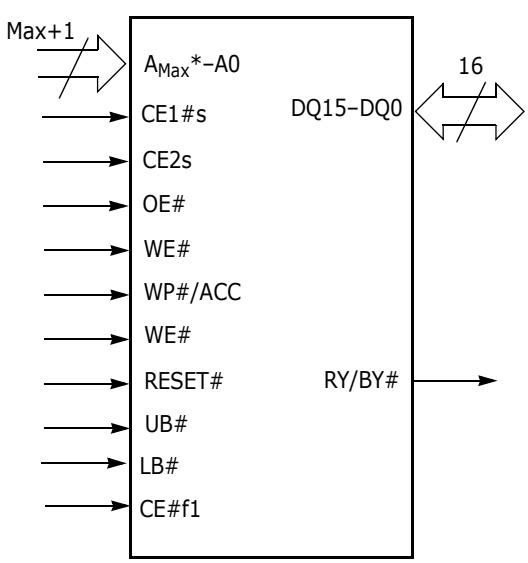



***Note:*** *Ball L5 (RFU) is a $V_{CC}$ on an 84-ball package; therefore, it is recommended that L5 not be connected to $V_{SS}$.*

## Input/Output Descriptions

| | | |
|---|---|---|
| A24-A0 | = | 25 Address inputs (512 Mb) |
| A23-A0 | = | 24 Address inputs (256 Mb) |
| A22-A0 | = | 23 Address inputs (128 Mb) |
| DQ15-DQ0 | = | Data input/output |
| OE# | = | Output Enable input. Asynchronous relative to CLK for the Burst mode. |
| WE# | = | Write Enable input. |
| $V_{SS}$ | = | Ground |
| NC | = | No Connect; not connected internally |
| RESET# | = | Hardware reset input. Low = device resets and returns to reading array data |
| WP#/ACC | = | Hardware write protect input / programming acceleration input. |
| CE1#s, CE2s | = | Chip-enable input for pSRAM. |
| CE#f1 | = | Chip-enable input for Flash 1. |
| $V_{CC}$f | = | Flash 3.0 Volt-only single power supply. |
| $V_{CC}$s | = | pSRAM Power Supply. |
| UB#s | = | Upper Byte Control (pSRAM). |
| LB#s | = | Lower Byte Control (pSRAM). |
| RFU | = | Reserved for future use. |
| RY/BY# | = | Ready/Busy output. |

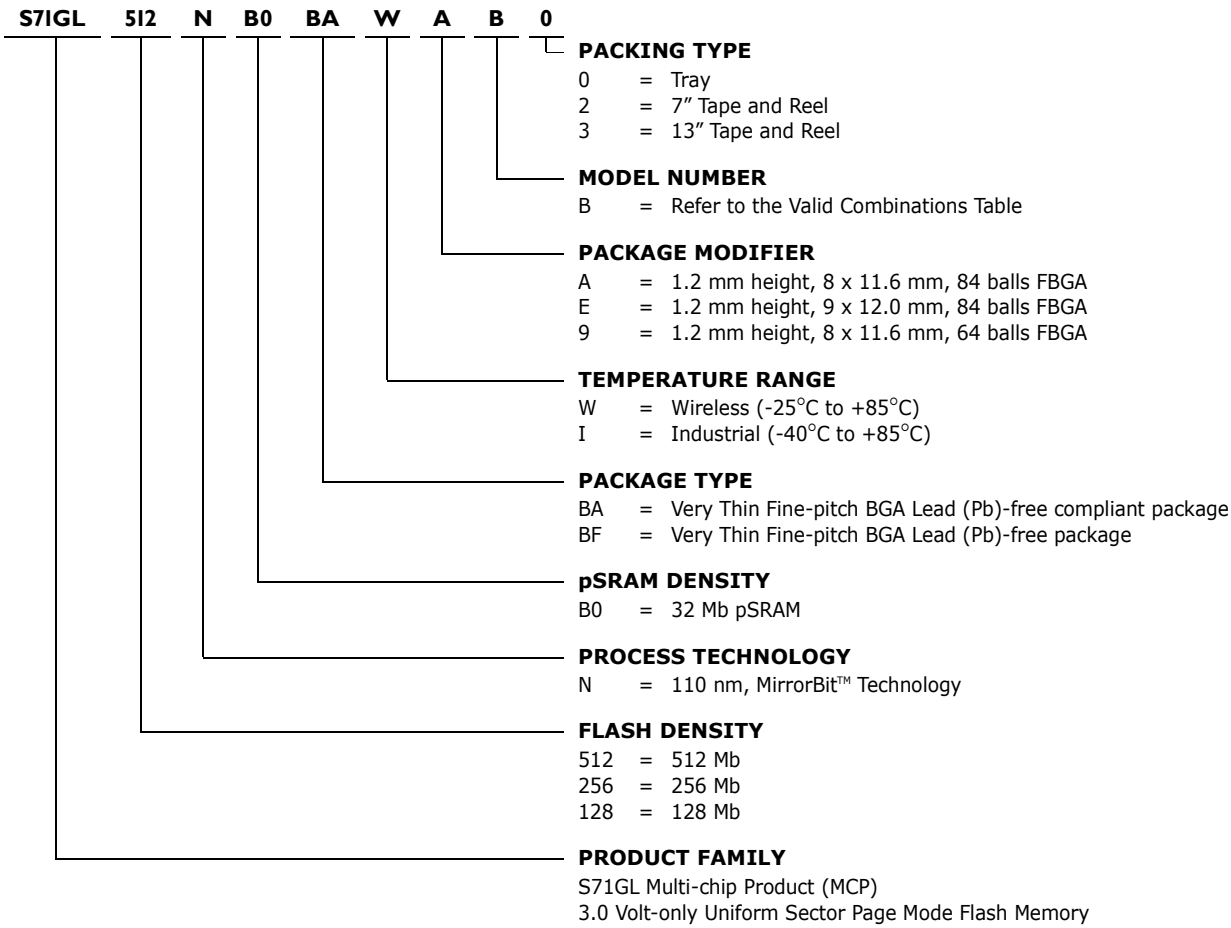
## Logic Symbol




*Max = A24

# Ordering Information

The order number (Valid Combination) is formed by the following:



| S71GL512NB0 Valid Combinations | | | | Flash Initial/Page Speed (ns) | Address Sector Protection | (p)SRAM Supplier | (p)SRAM Type/ Access Time (ns) | Package Type | Package Marking |
|---|---|---|---|---|---|---|---|---|---|
| Base Ordering Part Number | Package & Temperature | Package Modifier/ Model Number | Packing Type | | | | | | |
| S71GL512NB0 | BAW | EK | 0, 2, 3 (Note 1) | 105/25 | Lowest Add | Type 1 | 65/25 | 9mmx12mm 84-ball Lead (Pb)-free Compliant | (Note 2) |
| | | EP | | | Highest Add | | | | |
| | | EU | | | Lowest Add | Type 7 | | | |
| | | EZ | | | Highest Add | | | | |
| | | EJ | | 100/25 | Lowest Add | Type 1 | | | |
| | | EN | | | Highest Add | | | | |
| | | ET | | | Lowest Add | Type 7 | | | |
| | | EY | | | Highest Add | | | | |
| S71GL512NB0 | BFW | EK | 0, 2, 3 (Note 1) | 105/25 | Lowest Add | Type 1 | 65/25 | 9mmx12mm 84-ball Lead (Pb)-free | |
| | | EP | | | Highest Add | | | | |
| | | EU | | | Lowest Add | Type 7 | | | |
| | | EZ | | | Highest Add | | | | |
| | | EJ | | 100/25 | Lowest Add | Type 1 | | | |
| | | EN | | | Highest Add | | | | |
| | | ET | | | Lowest Add | Type 7 | | | |
| | | EY | | | Highest Add | | | | |

***Notes:***
1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S" and packing type designator from ordering part number.*

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

| S71GL256NB0 Valid Combinations | | | | Flash Initial/ Page Speed (ns) | Address Sector Protection | (p)SRAM Supplier | (p)SRAM Type/ Access Time (ns) | Package Type | Package Marking |
|---|---|---|---|---|---|---|---|---|---|
| Base Ordering Part Number | Package & Temperature | Package Modifier/ Model Number | Packing Type | | | | | | |
| S71GL256NB0 | BAW | AK | 0, 2, 3 (Note 1) | 100/25 | Lowest Add | Type 1 | 65/25 | 8mmx11.6mm 84-ball Lead (Pb)-free Compliant | (Note 2) |
| | | AP | | | Highest Add | | | | |
| | | AU | | | Lowest Add | Type 7 | | | |
| | | AZ | | | Highest Add | | | | |
| | | AJ | | 90/25 | Lowest Add | Type 1 | | | |
| | | AN | | | Highest Add | | | | |
| | | AT | | | Lowest Add | Type 7 | | | |
| | | AY | | | Highest Add | | | | |
| S71GL256NB0 | BFW | AK | 0, 2, 3 (Note 1) | 100/25 | Lowest Add | Type 1 | 65/25 | 8mmx11.6mm 84-ball Lead (Pb)-free | |
| | | AP | | | Highest Add | | | | |
| | | AU | | | Lowest Add | Type 7 | | | |
| | | AZ | | | Highest Add | | | | |
| | | AJ | | 90/25 | Lowest Add | Type 1 | | | |
| | | AN | | | Highest Add | | | | |
| | | AT | | | Lowest Add | Type 7 | | | |
| | | AY | | | Highest Add | | | | |

***Notes:***
1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S" and packing type designator from ordering part number.*

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

| S71GL128NB0 Valid Combinations | | | | Flash Initial/ Page Speed (ns) | Address Sector Protection | (p)SRAM Supplier | (p)SRAM Type/ Access Time (ns) | Package Type | Package Marking |
|---|---|---|---|---|---|---|---|---|---|
| Base Ordering Part Number | Package & Temperature | Package Modifier/ Model Number | Packing Type | | | | | | |
| S71GL128NB0 | BAW | 9K | 0, 2, 3 (Note 1) | 100/25 | Lowest Add | Type 1 | 65/25 | 8mmx11.6mm 64-ball Lead (Pb)-free Compliant | (Note 2) |
| | | 9P | | | Highest Add | | | | |
| | | 9U | | | Lowest Add | Type 7 | | | |
| | | 9Z | | | Highest Add | | | | |
| | | 9J | | 90/25 | Lowest Add | Type 1 | | | |
| | | 9N | | | Highest Add | | | | |
| | | 9T | | | Lowest Add | Type 7 | | | |
| | | 9Y | | | Highest Add | | | | |
| | | AK | | 100/25 | Lowest Add | Type 1 | | 8mmx11.6mm 84-ball Lead (Pb)-free Compliant | |
| | | AP | | | Highest Add | | | | |
| | | AU | | | Lowest Add | Type 7 | | | |
| | | AZ | | | Highest Add | | | | |
| | | AJ | | 90/25 | Lowest Add | Type 1 | | | |
| | | AN | | | Highest Add | | | | |
| | | AT | | | Lowest Add | Type 7 | | | |
| | | AY | | | Highest Add | | | | |
| S71GL128NB0 | BFW | 9K | 0, 2, 3 (Note 1) | 100/25 | Lowest Add | Type 1 | 65/25 | 8mmx11.6mm 64-ball Lead (Pb)-free Compliant | |
| | | 9P | | | Highest Add | | | | |
| | | 9U | | | Lowest Add | Type 7 | | | |
| | | 9Z | | | Highest Add | | | | |
| | | 9J | | 90/25 | Lowest Add | Type 1 | | | |
| | | 9N | | | Highest Add | | | | |
| | | 9T | | | Lowest Add | Type 7 | | | |
| | | 9Y | | | Highest Add | | | | |
| | | AK | | 100/25 | Lowest Add | Type 1 | | 8mmx11.6mm 84-ball Lead (Pb)-free | |
| | | AP | | | Highest Add | | | | |
| | | AU | | | Lowest Add | Type 7 | | | |
| | | AZ | | | Highest Add | | | | |
| | | AJ | | 90/25 | Lowest Add | Type 1 | | | |
| | | AN | | | Highest Add | | | | |
| | | AT | | | Lowest Add | Type 7 | | | |
| | | AY | | | Highest Add | | | | |

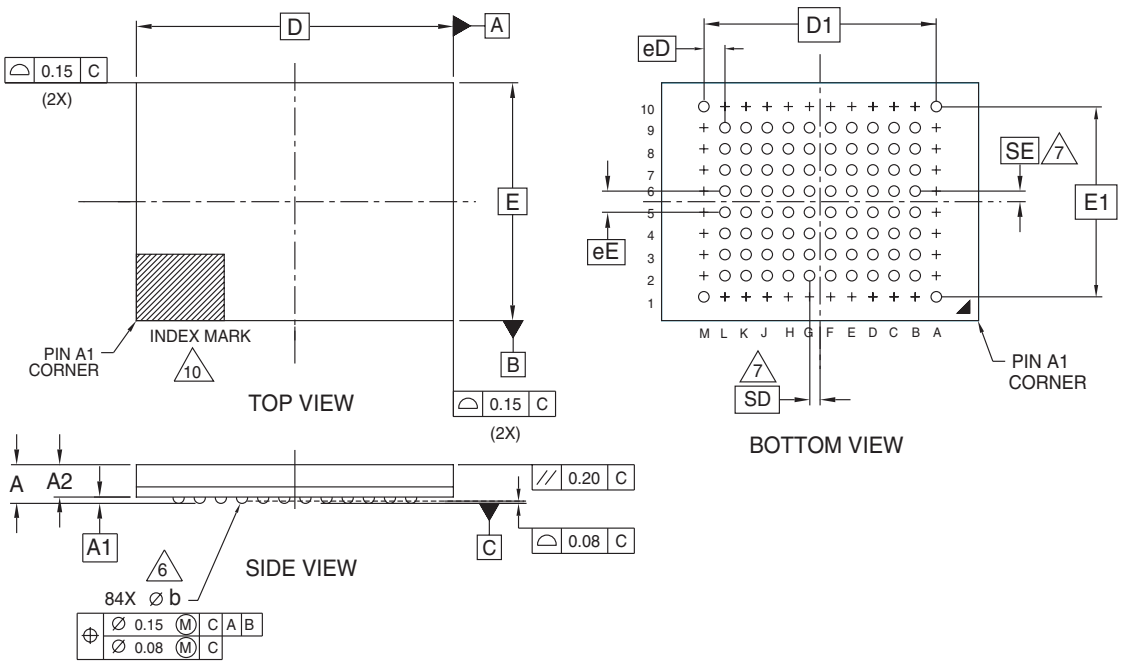
***Notes:***
1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S" and packing type designator from ordering part number.*

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

# Physical Dimensions

## TLD084—84-ball Fine-Pitch Ball Grid Array (FBGA) 9.0 x I2.0 xI.2 mm MCP Compatible Package




| PACKAGE | TLD 084 | | | |
|---|---|---|---|---|
| JEDEC | N/A | | | |
| D x E | 12.00 mm x 9.00 mm PACKAGE | | | |
| SYMBOL | MIN | NOM | MAX | NOTE |
| A | --- | --- | 1.20 | PROFILE |
| A1 | 0.17 | --- | --- | BALL HEIGHT |
| A2 | 0.81 | --- | 0.97 | BODY THICKNESS |
| D | | 12.00 BSC. | | BODY SIZE |
| E | | 9.00 BSC. | | BODY SIZE |
| D1 | | 8.80 BSC. | | MATRIX FOOTPRINT |
| E1 | | 7.20 BSC. | | MATRIX FOOTPRINT |
| MD | | 12 | | MATRIX SIZE D DIRECTION |
| ME | | 10 | | MATRIX SIZE E DIRECTION |
| n | | 84 | | BALL COUNT |
| b | 0.35 | 0.40 | 0.45 | BALL DIAMETER |
| eE | | 0.80 BSC. | | BALL PITCH |
| eD | | 0.80 BSC | | BALL PITCH |
| SD / SE | | 0.40 BSC. | | SOLDER BALL PLACEMENT |
| | | A2,A3,A4,A5,A6,A7,A8,A9 B1,B10,C1,C10,D1,D10 E1,E10,F1,F10,G1,G10 H1,H10,J1,J10,K1,K10 L1,L10,M2,M3,M4,M5,M6, M7,M8,M9 | | DEPOPULATED SOLDER BALLS |

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

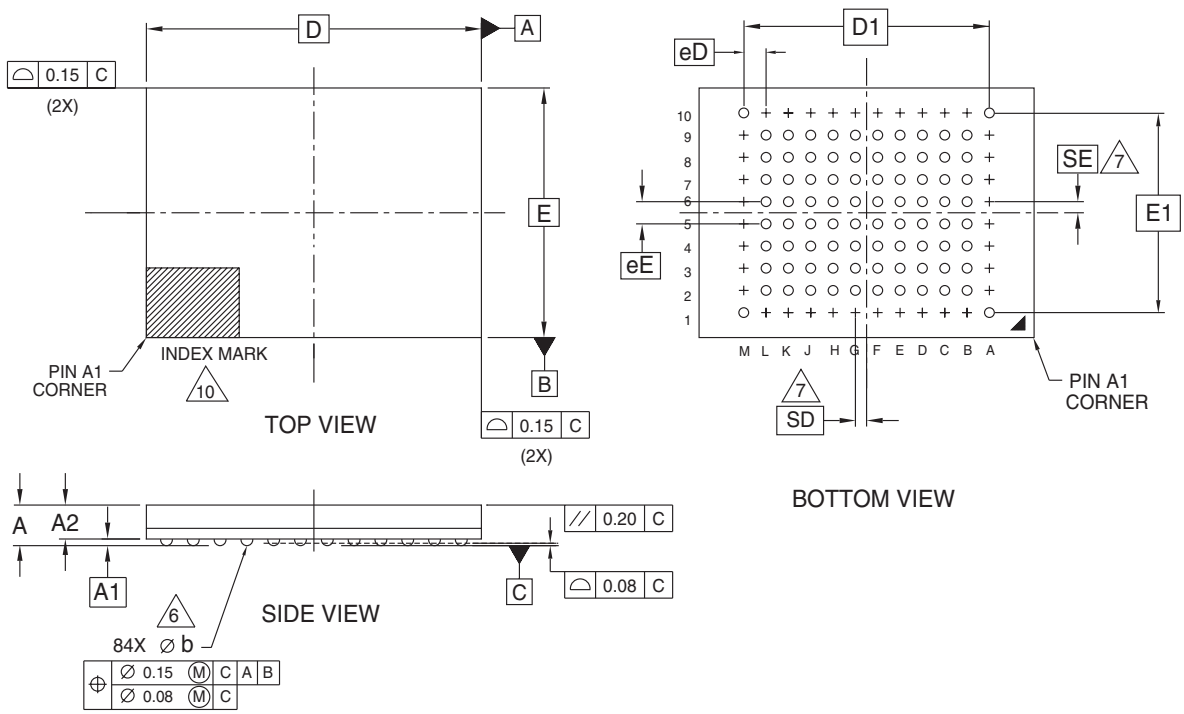
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3367\ 16-038.22a

***Note:*** *BSC is an ANSI standard for Basic Space Centering*

## TLA084—84-ball Fine-Pitch Ball Grid Array (FBGA) 8.0 x 11.6 x1.2 mm MCP Compatible Package




| PACKAGE | TLA 084 | | | |
|---|---|---|---|---|
| JEDEC | N/A | | | |
| D x E | 11.60 mm x 8.00 mm PACKAGE | | | |
| SYMBOL | MIN | NOM | MAX | NOTE |
| A | --- | --- | 1.20 | PROFILE |
| A1 | 0.17 | --- | --- | BALL HEIGHT |
| A2 | 0.81 | --- | 0.97 | BODY THICKNESS |
| D | 11.60 BSC. | | | BODY SIZE |
| E | 8.00 BSC. | | | BODY SIZE |
| D1 | 8.80 BSC. | | | MATRIX FOOTPRINT |
| E1 | 7.20 BSC. | | | MATRIX FOOTPRINT |
| MD | 12 | | | MATRIX SIZE D DIRECTION |
| ME | 10 | | | MATRIX SIZE E DIRECTION |
| n | 84 | | | BALL COUNT |
| Ø b | 0.35 | 0.40 | 0.45 | BALL DIAMETER |
| eE | 0.80 BSC. | | | BALL PITCH |
| eD | 0.80 BSC | | | BALL PITCH |
| SD / SE | 0.40 BSC. | | | SOLDER BALL PLACEMENT |
| | A2,A3,A4,A5,A6,A7,A8,A9 B1,B10,C1,C10,D1,D10, E1,E10,F1,F10,G1,G10, H1,H10,J1,J10,K1,K10,L1,L10, M2,M3,M4,M5,M6,M7,M8,M9 | | | DEPOPULATED SOLDER BALLS |

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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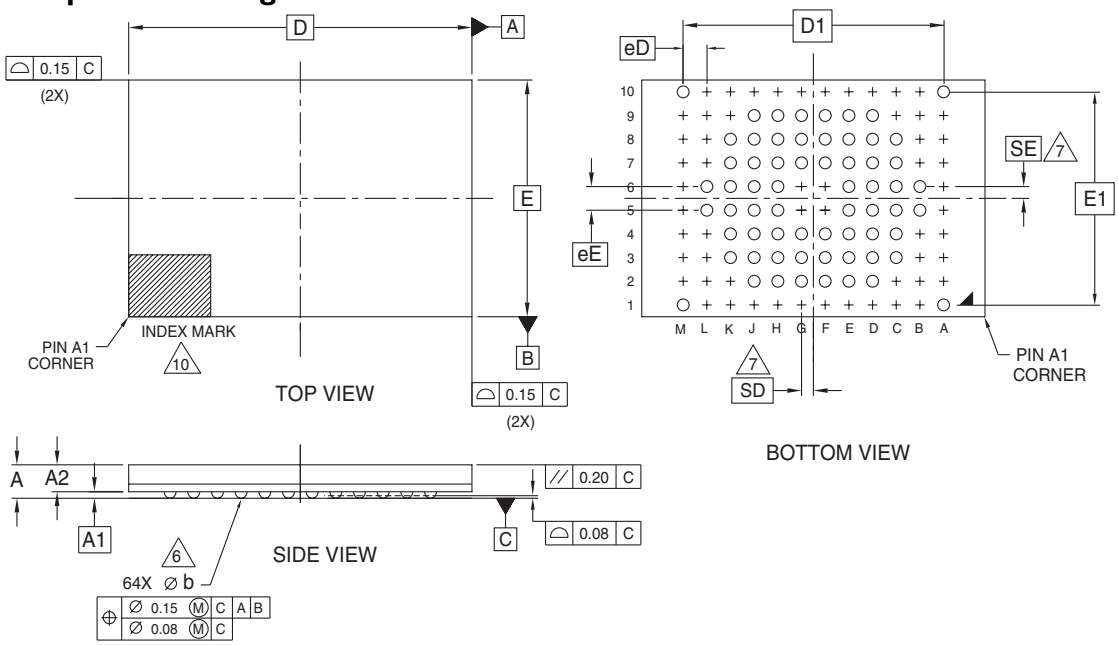
***Note:*** *BSC is an ANSI standard for Basic Space Centering*

## TLA064—64-ball Fine-Pitch Ball Grid Array (FBGA) 8.0 x 11.6 xl.2 mm MCP Compatible Package




| PACKAGE | TLA 064 | | | |
|---|---|---|---|---|
| JEDEC | N/A | | | |
| D x E | 11.60 mm x 8.00 mm PACKAGE | | | |
| SYMBOL | MIN | NOM | MAX | NOTE |
| A | --- | --- | 1.20 | PROFILE |
| A1 | 0.17 | --- | --- | BALL HEIGHT |
| A2 | 0.81 | --- | 0.97 | BODY THICKNESS |
| D | | 11.60 BSC. | | BODY SIZE |
| E | | 8.00 BSC. | | BODY SIZE |
| D1 | | 8.80 BSC. | | MATRIX FOOTPRINT |
| E1 | | 7.20 BSC. | | MATRIX FOOTPRINT |
| MD | | 12 | | MATRIX SIZE D DIRECTION |
| ME | | 10 | | MATRIX SIZE E DIRECTION |
| n | | 64 | | BALL COUNT |
| ϕb | 0.35 | 0.40 | 0.45 | BALL DIAMETER |
| eE | | 0.80 BSC. | | BALL PITCH |
| eD | | 0.80 BSC | | BALL PITCH |
| SD / SE | | 0.40 BSC. | | SOLDER BALL PLACEMENT |
| | A2,A3,A4,A5,A6,A7,A8,A9 B1,B2,B3,B4,B7,B8,B9,B10 C1,C2,C9,C10,D1,D10,E1,E10, F1,F5,F6,F10,G1,G5,G6,G10 H1,H10,J1,J10,K1,K2,K9,K10 L1,L2,L3,L4,L7,L8,L9,L10 M2,M3,M4,M5,M6,M7,M8,M9 | | | DEPOPULATED SOLDER BALLS |

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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***Note:*** *BSC is an ANSI standard for Basic Space Centering.*

# S29GLxxxN MirrorBit™ Flash Family
## S29GL512N, S29GL256N, S29GL128N
**512 Megabit, 256 Megabit, and 128 Megabit,**
**3.0 Volt-only Page Mode Flash Memory featuring**
**110 nm MirrorBit process technology**

SPANSION™

## Datasheet

**ADVANCE INFORMATION**

# Distinctive Characteristics

## Architectural Advantages

- **Single power supply operation**
  - 3 volt read, erase, and program operations
- **Enhanced VersatileI/O™ control**
  - All input levels (address, control, and DQ input levels) and outputs are determined by voltage on $V_{IO}$ input. $V_{IO}$ range is 1.65 to $V_{CC}$
- **Manufactured on 110 nm MirrorBit process technology**
- **Secured Silicon Sector region**
  - 128-word/256-byte sector for permanent, secure identification through an 8-word/16-byte random Electronic Serial Number, accessible through a command sequence
  - May be programmed and locked at the factory or by the customer
- **Flexible sector architecture**
  - S29GL512N: Five hundred twelve 64 Kword (128 Kbyte) sectors
  - S29GL256N: Two hundred fifty-six 64 Kword (128 Kbyte) sectors
  - S29GL128N: One hundred twenty-eight 64 Kword (128 Kbyte) sectors
- **Compatibility with JEDEC standards**
  - Provides pinout and software compatibility for single-power supply flash, and superior inadvertent write protection
- **100,000 erase cycles per sector typical**
- **20-year data retention typical**

## Performance Characteristics

- **High performance**
  - 80 ns access time (S29GL128N, S29GL256N), 90 ns access time (S29GL512N)
  - 8-word/16-byte page read buffer
  - 25 ns page read times
  - 16-word/32-byte write buffer reduces overall programming time for multiple-word updates
- **Low power consumption (typical values at 3.0 V, 5 MHz)**
  - 25 mA typical active read current;
  - 50 mA typical erase/program current
  - 1 µA typical standby mode current

## Software & Hardware Features

- **Software features**
  - Program Suspend & Resume: read other sectors before programming operation is completed
  - Erase Suspend & Resume: read/program other sectors before an erase operation is completed
  - Data# polling & toggle bits provide status
  - Unlock Bypass Program command reduces overall multiple-word or byte programming time
  - CFI (Common Flash Interface) compliant: allows host system to identify and accommodate multiple flash devices
- **Hardware features**
  - Advanced Sector Protection
  - WP#/ACC input accelerates programming time (when high voltage is applied) for greater throughput during system production. Protects first or last sector regardless of sector protection settings
  - Hardware reset input (RESET#) resets device
  - Ready/Busy# output (RY/BY#) detects program or erase cycle completion

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# General Description

The GL512/256/128N family of devices are 3.0V single power flash memory manufactured using 110 nm MirrorBit technology. The GL512N is a 512 Mbit, organized as 33,554,432 words or 67,108,864 bytes. The GL256N is a 256 Mbit, organized as 16,777,216 words or 33,554,432 bytes. The GL128N is a 128 Mbit, organized as 8,388,608 words or 16,777,216 bytes. The devices have a 16-bit wide data bus that can also function as an 8-bit wide data bus by using the BYTE# input. The device can be programmed either in the host system or in standard EPROM programmers.

Access times as fast as 90 ns (GL128N, GL256N) or 100 ns (GL512N) are available.

Each device requires only a **single 3.0 volt power supply** for both read and write functions. In addition to a $V_{CC}$ input, a high-voltage **accelerated program (**WP#/**ACC)** input provides shorter programming times through increased current. This feature is intended to facilitate factory throughput during system production, but may also be used in the field if desired.

The devices are entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the device using standard microprocessor write timing. Write cycles also internally latch addresses and data needed for the programming and erase operations.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Device programming and erasure are initiated through command sequences. Once a program or erase operation has begun, the host system need only poll the DQ7 (Data# Polling) or DQ6 (toggle) **status bits** or monitor the **Ready/Busy# (RY/BY#)** output to determine whether the operation is complete. To facilitate programming, an **Unlock Bypass** mode reduces command sequence overhead by requiring only two write cycles to program data instead of four.

**Hardware data protection** measures include a low $V_{CC}$ detector that automatically inhibits write operations during power transitions. **Persistent Sector Protection** provides in-system, command-enabled protection of any combination of sectors using a single power supply at $V_{CC}$. **Password Sector Protection** prevents unauthorized write and erase operations in any combination of sectors through a user-defined 64-bit password.

The **Erase Suspend/Erase Resume** feature allows the host system to pause an erase operation in a given sector to read or program any other sector and then complete the erase operation. The **Program Suspend/Program Resume** feature enables the host system to pause a program operation in a given sector to read any other sector and then complete the program operation.

The **hardware RESET# pin** terminates any operation in progress and resets the device, after which it is then ready for a new operation. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the host system to read boot-up firmware from the Flash memory device.

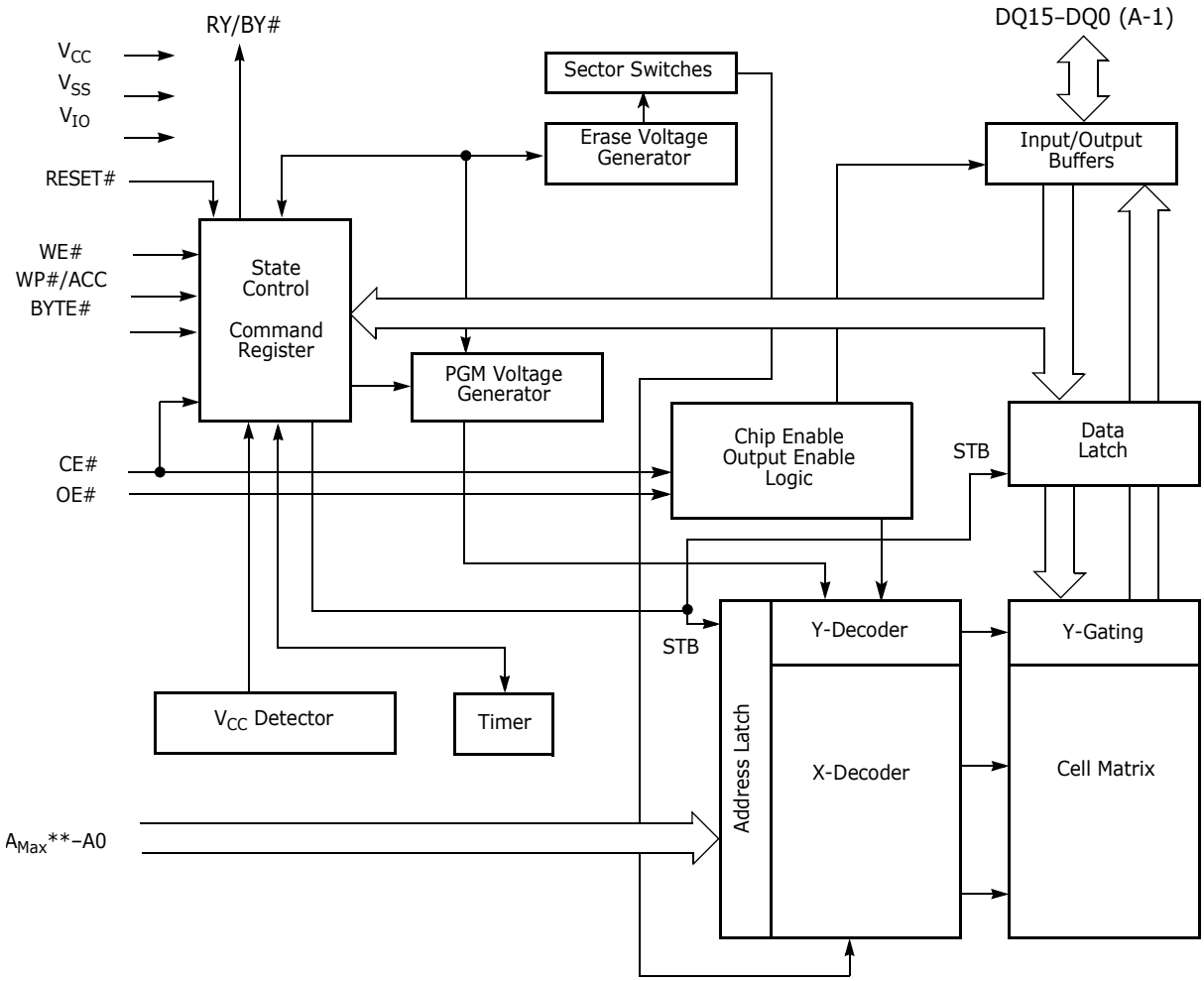
The device reduces power consumption in the **standby mode** when it detects specific voltage levels on CE# and RESET#, or when addresses have been stable for a specified period of time.

The **Secured Silicon Sector** provides a 128-word/256-byte area for code or data that can be permanently protected. Once this sector is protected, no further changes within the sector can occur.

The **Write Protect (WP#/ACC)** feature protects the first or last sector by asserting a logic low on the WP# pin.

MirrorBit flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via hot-hole assisted erase. The data is programmed using hot electron injection.

## Block Diagram



# Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

**Table 1. Device Bus Operations**

| Operation | CE# | OE# | WE# | RESET# | WP# | ACC | Addresses (Note 2) | DQ0–DQ7 | DQ8–DQ15 | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | BYTE# = $V_{IH}$ | BYTE# = $V_{IL}$ |
| Read | L | L | H | H | X | X | $A_{IN}$ | $D_{OUT}$ | $D_{OUT}$ | DQ8–DQ14 = High-Z, DQ15 = A-1 |
| Write (Program/Erase) | L | H | L | H | (Note 2) | X | $A_{IN}$ | (Note 3) | (Note 3) | |
| Accelerated Program | L | H | L | H | (Note 2) | $V_{HH}$ | $A_{IN}$ | (Note 3) | (Note 3) | |
| Standby | $V_{CC}$ ± 0.3 V | X | X | $V_{CC}$ ± 0.3 V | X | H | X | High-Z | High-Z | High-Z |
| Output Disable | L | H | H | H | X | X | X | High-Z | High-Z | High-Z |
| Reset | X | X | X | L | X | X | X | High-Z | High-Z | High-Z |

***Legend:*** *L = Logic Low = $V_{IL}$, H = Logic High = $V_{IH}$, $V_{ID}$ = 11.5–12.5 V, $V_{HH}$ = 11.5–12.5V, X = Don't Care, SA = Sector Address, $A_{IN}$ = Address In, $D_{IN}$ = Data In, $D_{OUT}$ = Data Out*

***Notes:***

1. *Addresses are AMax:A0 in word mode; $A_{Max}$:A-1 in byte mode. Sector addresses are $A_{Max}$:A16 in both modes.*
2. *If WP# = $V_{IL}$, the first or last sector group remains protected. If WP# = $V_{IH}$, the first or last sector will be protected or unprotected as determined by the method described in "Write Protect (WP#)". All sectors are unprotected when shipped from the factory (The Secured Silicon Sector may be factory protected depending on version ordered.)*
3. *$D_{IN}$ or $D_{OUT}$ as required by command sequence, data polling, or sector protect algorithm (see Figure 2).*

## Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins operate in the byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, DQ0–DQ15 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

## Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to $V_{IL}$. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at $V_{IH}$.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read-Only Operations table for timing specifications and to Figure 11 for the timing diagram. Refer to the DC Characteristics table for the active current specification on reading array data.

### Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The page size of the device is 8 words/16 bytes. The appropriate page is selected by the higher address bits A(max)–A3. Address bits A2–A0 in word mode (A2–A-1 in byte mode) determine the specific word within a page. This is an asynchronous operation; the microprocessor supplies the specific word location.

The random or initial page access is equal to $t_{ACC}$ or $t_{CE}$ and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to $t_{PACC}$. When CE# is de-asserted and reasserted for a subsequent access, the access time is $t_{ACC}$ or $t_{CE}$. Fast page mode accesses are obtained by keeping the "read-page addresses" constant and changing the "intra-read page" addresses.

## Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to $V_{IL}$, and OE# to $V_{IH}$.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The "Word/Byte Program Command Sequence" section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 2 indicates the address space that each sector occupies.

Refer to the DC Characteristics table for the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

### Write Buffer

Write Buffer Programming allows the system write to a maximum of 16 words/32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. See "Write Buffer" for more information.

### Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the WP#/ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts $V_{HH}$ on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sector groups, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing $V_{HH}$ from the WP#/ACC pin returns the device to normal operation. *Note that the WP#/ACC pin must not be at $V_{HH}$ for operations other than accelerated programming, or device damage may result. WP# has an internal pullup; when unconnected, WP# is at $V_{IH}$.*

### Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the "Autoselect Command Sequence" section on page 50 sections for more information.

## Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{IO} \pm 0.3$ V. (Note that this is a more restricted voltage range than $V_{IH}$.) If CE# and RESET# are held at $V_{IH}$, but not within $V_{IO} \pm 0.3$ V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time ($t_{CE}$) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

Refer to the "DC Characteristics" section on page 78 for the standby current specification.

## Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for $t_{ACC}$ + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Refer to the "DC Characteristics" section on page 78 for the automatic sleep mode current specification.

## RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of $t_{RP}$, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The op-

eration that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS}$±0.3 V, the device draws CMOS standby current ($I_{CC5}$). If RESET# is held at $V_{IL}$ but not within $V_{SS}$±0.3 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 13 for the timing diagram.

## Output Disable Mode

When the OE# input is at $V_{IH}$, output from the device is disabled. The output pins are placed in the high impedance state.

**Table 2. Sector Address Table–S29GL256N**

| Sector | A23–A16 | | | | | | | | Sector Size (Kbytes/ Kwords) | 8-bit Address Range (in hexadecimal) | 16-bit Address Range (in hexadecimal) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 128/64 | 0000000–001FFFF | 0000000–000FFFF |
| SA1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 128/64 | 0020000–003FFFF | 0010000–001FFFF |
| SA2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 128/64 | 0040000–005FFFF | 0020000–002FFFF |
| SA3 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 128/64 | 0060000–007FFFF | 0030000–003FFFF |
| SA4 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 128/64 | 0080000–009FFFF | 0040000–004FFFF |
| SA5 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 128/64 | 00A0000–00BFFFF | 0050000–005FFFF |
| SA6 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 128/64 | 00C0000–00DFFFF | 0060000–006FFFF |
| SA7 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 128/64 | 00E0000–00FFFFF | 0070000–007FFFF |
| SA8 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 128/64 | 0100000–011FFFF | 0080000–008FFFF |
| SA9 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 128/64 | 0120000–013FFFF | 0090000–009FFFF |
| SA10 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 128/64 | 0140000–015FFFF | 00A0000–00AFFFF |
| SA11 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 128/64 | 0160000–017FFFF | 00B0000–00BFFFF |
| SA12 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 128/64 | 0180000–019FFFF | 00C0000–00CFFFF |
| SA13 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 128/64 | 01A0000–01BFFFF | 00D0000–00DFFFF |
| SA14 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 128/64 | 01C0000–01DFFFF | 00E0000–00EFFFF |
| SA15 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 128/64 | 01E0000–01FFFFF | 00F0000–00FFFFF |
| SA16 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 128/64 | 0200000–021FFFF | 0100000–010FFFF |
| SA17 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 128/64 | 0220000–023FFFF | 0110000–011FFFF |
| SA18 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 128/64 | 0240000–025FFFF | 0120000–012FFFF |
| SA19 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 128/64 | 0260000–027FFFF | 0130000–013FFFF |
| SA20 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 128/64 | 0280000–029FFFF | 0140000–014FFFF |
| SA21 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 128/64 | 02A0000–02BFFFF | 0150000–015FFFF |
| SA22 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 128/64 | 02C0000–02DFFFF | 0160000–016FFFF |

## Table 2. Sector Address Table–S29GL256N (Continued)

| Sector | A23–A16 | | | | | | | | Sector Size (Kbytes/ Kwords) | 8-bit Address Range (in hexadecimal) | 16-bit Address Range (in hexadecimal) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SA23 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 128/64 | 02E0000–02FFFFF | 0170000–017FFFF |
| SA24 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 128/64 | 0300000–031FFFF | 0180000–018FFFF |
| SA25 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 128/64 | 0320000–033FFFF | 0190000–019FFFF |
| SA26 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 128/64 | 0340000–035FFFF | 01A0000–01AFFFF |
| SA27 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 128/64 | 0360000–037FFFF | 01B0000–01BFFFF |
| SA28 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 128/64 | 0380000–039FFFF | 01C0000–01CFFFF |
| SA29 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 128/64 | 03A0000–03BFFFF | 01D0000–01DFFFF |
| SA30 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 128/64 | 03C0000–03DFFFF | 01E0000–01EFFFF |
| SA31 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 128/64 | 03E0000–03FFFFF | 01F0000–01FFFFF |
| SA32 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 128/64 | 0400000–041FFFF | 0200000–020FFFF |
| SA33 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 128/64 | 0420000–043FFFF | 0210000–021FFFF |
| SA34 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 128/64 | 0440000–045FFFF | 0220000–022FFFF |
| SA35 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 128/64 | 0460000–047FFFF | 0230000–023FFFF |
| SA36 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 128/64 | 0480000–049FFFF | 0240000–024FFFF |
| SA37 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 128/64 | 04A0000–04BFFFF | 0250000–025FFFF |
| SA38 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 128/64 | 04C0000–04DFFFF | 0260000–026FFFF |
| SA39 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 128/64 | 04E0000–04FFFFF | 0270000–027FFFF |
| SA40 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 128/64 | 0500000–051FFFF | 0280000–028FFFF |
| SA41 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 128/64 | 0520000–053FFFF | 0290000–029FFFF |
| SA42 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 128/64 | 0540000–055FFFF | 02A0000–02AFFFF |
| SA43 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 128/64 | 0560000–057FFFF | 02B0000–02BFFFF |
| SA44 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 128/64 | 0580000–059FFFF | 02C0000–02CFFFF |
| SA45 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 128/64 | 05A0000–05BFFFF | 02D0000–02DFFFF |
| SA46 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 128/64 | 05C0000–05DFFFF | 02E0000–02EFFFF |
| SA47 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 128/64 | 05E0000–05FFFFF | 02F0000–02FFFFF |
| SA48 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 128/64 | 0600000–061FFFF | 0300000–030FFFF |
| SA49 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 128/64 | 0620000–063FFFF | 0310000–031FFFF |
| SA50 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 128/64 | 0640000–065FFFF | 0320000–032FFFF |
| SA51 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 128/64 | 0660000–067FFFF | 0330000–033FFFF |
| SA52 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 128/64 | 0680000–069FFFF | 0340000–034FFFF |
| SA53 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 128/64 | 06A0000–06BFFFF | 0350000–035FFFF |
| SA54 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 128/64 | 06C0000–06DFFFF | 0360000–036FFFF |
| SA55 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 128/64 | 06E0000–06FFFFF | 0370000–037FFFF |
| SA56 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 128/64 | 0700000–071FFFF | 0380000–038FFFF |
| SA57 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 128/64 | 0720000–073FFFF | 0390000–039FFFF |

**Table 2. Sector Address Table–S29GL256N (Continued)**

| Sector | A23–A16 | | | | | | | | Sector Size (Kbytes/ Kwords) | 8-bit Address Range (in hexadecimal) | 16-bit Address Range (in hexadecimal) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SA58 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 128/64 | 0740000–075FFFF | 03A0000–03AFFFF |
| SA59 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 128/64 | 0760000–077FFFF | 03B0000–03BFFFF |
| SA60 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 128/64 | 0780000–079FFFF | 03C0000–03CFFFF |
| SA61 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 128/64 | 07A0000–7BFFFF | 03D0000–03DFFFF |
| SA62 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 128/64 | 07C0000–07DFFFF | 03E0000–03EFFFF |
| SA63 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 128/64 | 07E0000–07FFFF0 | 03F0000–03FFFF |
| SA64 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 128/64 | 0800000–081FFFF | 0400000–040FFFF |
| SA65 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 128/64 | 0820000–083FFFF | 0410000–041FFFF |
| SA66 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 128/64 | 0840000–085FFFF | 0420000–042FFFF |
| SA67 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 128/64 | 0860000–087FFFF | 0430000–043FFFF |
| SA68 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 128/64 | 0880000–089FFFF | 0440000–044FFFF |
| SA69 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 128/64 | 08A0000–08BFFFF | 0450000–045FFFF |
| SA70 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 128/64 | 08C0000–08DFFFF | 0460000–046FFFF |
| SA71 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 128/64 | 08E0000–08FFFFF | 0470000–047FFFF |
| SA72 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 128/64 | 0900000–091FFFF | 0480000–048FFFF |
| SA73 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 128/64 | 0920000–093FFFF | 0490000–049FFFF |
| SA74 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 128/64 | 0940000–095FFFF | 04A0000–04AFFFF |
| SA75 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 128/64 | 0960000–097FFFF | 04B0000–04BFFFF |
| SA76 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 128/64 | 0980000–099FFFF | 04C0000–04CFFFF |
| SA77 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 128/64 | 09A0000–09BFFFF | 04D0000–04DFFFF |
| SA78 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 128/64 | 09C0000–09DFFFF | 04E0000–04EFFFF |
| SA79 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 128/64 | 09E0000–09FFFFF | 04F0000–04FFFFF |
| SA80 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 128/64 | 0A00000–0A1FFFF | 0500000–050FFFF |
| SA81 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 128/64 | 0A20000–0A3FFFF | 0510000–051FFFF |
| SA82 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 128/64 | 0A40000–045FFFF | 0520000–052FFFF |
| SA83 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 128/64 | 0A60000–0A7FFFF | 0530000–053FFFF |
| SA84 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 128/64 | 0A80000–0A9FFFF | 0540000–054FFFF |
| SA85 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 128/64 | 0AA0000–0ABFFFF | 0550000–055FFFF |
| SA86 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 128/64 | 0AC0000–0ADFFFF | 0560000–056FFFF |
| SA87 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 128/64 | 0AE0000–AEFFFFF | 0570000–057FFFF |
| SA88 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 128/64 | 0B00000–0B1FFFF | 0580000–058FFFF |
| SA89 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 128/64 | 0B20000–0B3FFFF | 0590000–059FFFF |
| SA90 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 128/64 | 0B40000–0B5FFFF | 05A0000–05AFFFF |
| SA91 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 128/64 | 0B60000–0B7FFFF | 05B0000–05BFFFF |
| SA92 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 128/64 | 0B80000–0B9FFFF | 05C0000–05CFFFF |

## Table 2. Sector Address Table–S29GL256N (Continued)

| Sector | A23–A16 | | | | | | | | Sector Size (Kbytes/ Kwords) | 8-bit Address Range (in hexadecimal) | 16-bit Address Range (in hexadecimal) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SA93 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 128/64 | 0BA0000–0BBFFFF | 05D0000–05DFFFF |
| SA94 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 128/64 | 0BC0000–0BDFFFF | 05E0000–05EFFFF |
| SA95 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 128/64 | 0BE0000–0BFFFFF | 05F0000–05FFFFF |
| SA96 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 128/64 | 0C00000–0C1FFFF | 0600000–060FFFF |
| SA97 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 128/64 | 0C20000–0C3FFFF | 0610000–061FFFF |
| SA98 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 128/64 | 0C40000–0C5FFFF | 0620000–062FFFF |
| SA99 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 128/64 | 0C60000–0C7FFFF | 0630000–063FFFF |
| SA100 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 128/64 | 0C80000–0C9FFFF | 0640000–064FFFF |
| SA101 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 128/64 | 0CA0000–0CBFFFF | 0650000–065FFFF |
| SA102 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 128/64 | 0CC0000–0CDFFFF | 0660000–066FFFF |
| SA103 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 128/64 | 0CE0000–0CFFFFF | 0670000–067FFFF |
| SA104 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 128/64 | 0D00000–0D1FFFF | 0680000–068FFFF |
| SA105 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 128/64 | 0D20000–0D3FFFF | 0690000–069FFFF |
| SA106 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 128/64 | 0D40000–0D5FFFF | 06A0000–06AFFFF |
| SA107 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 128/64 | 0D60000–0D7FFFF | 06B0000–06BFFFF |
| SA108 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 128/64 | 0D80000–0D9FFFF | 06C0000–06CFFFF |
| SA109 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 128/64 | 0DA0000–0DBFFFF | 06D0000–06DFFFF |
| SA110 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 128/64 | 0DC0000–0DDFFFF | 06E0000–06EFFFF |
| SA111 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 128/64 | 0DE0000–0DFFFFF | 06F0000–06FFFFF |
| SA112 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 128/64 | 0E00000–0E1FFFF | 0700000–070FFFF |
| SA113 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 128/64 | 0E20000–0E3FFFF | 0710000–071FFFF |
| SA114 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 128/64 | 0E40000–0E5FFFF | 0720000–072FFFF |
| SA115 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 128/64 | 0E60000–0E7FFFF | 0730000–073FFFF |
| SA116 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 128/64 | 0E80000–0E9FFFF | 0740000–074FFFF |
| SA117 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 128/64 | 0EA0000–0EBFFFF | 0750000–075FFFF |
| SA118 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 128/64 | 0EC0000–0EDFFFF | 0760000–076FFFF |
| SA119 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 128/64 | 0EE0000–0EFFFFF | 0770000–077FFFF |
| SA120 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 128/64 | 0F00000–0F1FFFF | 0780000–078FFFF |
| SA121 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 128/64 | 0F20000–0F3FFFF | 0790000–079FFFF |
| SA122 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 128/64 | 0F40000–0F5FFFF | 07A0000–07AFFFF |
| SA123 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 128/64 | 0F60000–0F7FFFF | 07B0000–07BFFFF |
| SA124 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 128/64 | 0F80000–0F9FFFF | 07C0000–07CFFFF |
| SA125 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 128/64 | 0FA0000–0FBFFFF | 07D0000–07DFFFF |
| SA126 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 128/64 | 0FC0000–0FDFFFF | 07E0000–07EFFFF |
| SA127 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 128/64 | 0FE0000–0FFFFFF | 07F0000–07FFFFF |

**Table 2. Sector Address Table–S29GL256N (Continued)**

| Sector | A23–A16 | | | | | | | | Sector Size (Kbytes/ Kwords) | 8-bit Address Range (in hexadecimal) | 16-bit Address Range (in hexadecimal) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SA128 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 128/64 | 1000000–101FFFF | 0800000–080FFFF |
| SA129 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 128/64 | 1020000–103FFFF | 0810000–081FFFF |
| SA130 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 128/64 | 1040000–105FFFF | 0820000–082FFFF |
| SA131 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 128/64 | 1060000–107FFFF | 0830000–083FFFF |
| SA132 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 128/64 | 1080000–109FFFF | 0840000–084FFFF |
| SA133 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 128/64 | 10A0000–10BFFFF | 0850000–085FFFF |
| SA134 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 128/64 | 10C0000–10DFFFF | 0860000–086FFFF |
| SA135 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 128/64 | 10E0000–10FFFFF | 0870000–087FFFF |
| SA136 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 128/64 | 1100000–111FFFF | 0880000–088FFFF |
| SA137 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 128/64 | 1120000–113FFFF | 0890000–089FFFF |
| SA138 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 128/64 | 1140000–115FFFF | 08A0000–08AFFFF |
| SA139 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 128/64 | 1160000–117FFFF | 08B0000–08BFFFF |
| SA140 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 128/64 | 1180000–119FFFF | 08C0000–08CFFFF |
| SA141 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 128/64 | 11A0000–11BFFFF | 08D0000–08DFFFF |
| SA142 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 128/64 | 11C0000–11DFFFF | 08E0000–08EFFFF |
| SA143 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 128/64 | 11E0000–11FFFFF | 08F0000–08FFFFF |
| SA144 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 128/64 | 1200000–121FFFF | 0900000–090FFFF |
| SA145 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 128/64 | 1220000–123FFFF | 0910000–091FFFF |
| SA146 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 128/64 | 1240000–125FFFF | 0920000–092FFFF |
| SA147 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 128/64 | 1260000–127FFFF | 0930000–093FFFF |
| SA148 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 128/64 | 1280000–129FFFF | 0940000–094FFFF |
| SA149 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 128/64 | 12A0000–12BFFFF | 0950000–095FFFF |
| SA150 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 128/64 | 12C0000–12DFFFF | 0960000–096FFFF |
| SA151 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 128/64 | 12E0000–12FFFFF | 0970000–097FFFF |
| SA152 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 128/64 | 1300000–131FFFF | 0980000–098FFFF |
| SA153 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 128/64 | 1320000–133FFFF | 0990000–099FFFF |
| SA154 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 128/64 | 1340000–135FFFF | 09A0000–09AFFFF |
| SA155 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 128/64 | 1360000–137FFFF | 09B0000–09BFFFF |
| SA156 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 128/64 | 1380000–139FFFF | 09C0000–09CFFFF |
| SA157 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 128/64 | 13A0000–13BFFFF | 09D0000–09DFFFF |
| SA158 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 128/64 | 13C0000–13DFFFF | 09E0000–09EFFFF |
| SA159 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 128/64 | 13E0000–13FFFFF | 09F0000–09FFFFF |
| SA160 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 128/64 | 1400000–141FFFF | 0A00000–0A0FFFF |
| SA161 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 128/64 | 1420000–143FFFF | 0A10000–0A1FFFF |
| SA162 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 128/64 | 1440000–145FFFF | 0A20000–0A2FFFF |

## Table 2. Sector Address Table–S29GL256N (Continued)

| Sector | A23–A16 | | | | | | | | Sector Size (Kbytes/ Kwords) | 8-bit Address Range (in hexadecimal) | 16-bit Address Range (in hexadecimal) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SA163 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 128/64 | 1460000–147FFFF | 0A30000–0A3FFFF |
| SA164 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 128/64 | 1480000–149FFFF | 0A40000–0A4FFFF |
| SA165 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 128/64 | 14A0000–14BFFFF | 0A50000–0A5FFFF |
| SA166 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 128/64 | 14C0000–14DFFFF | 0A60000–0A6FFFF |
| SA167 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 128/64 | 14E0000–14FFFFF | 0A70000–0A7FFFF |
| SA168 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 128/64 | 1500000–151FFFF | 0A80000–0A8FFFF |
| SA169 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 128/64 | 1520000–153FFFF | 0A90000–0A9FFFF |
| SA170 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 128/64 | 1540000–155FFFF | 0AA0000–0AAFFFF |
| SA171 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 128/64 | 1560000–157FFFF | 0AB0000–0ABFFFF |
| SA172 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 128/64 | 1580000–159FFFF | 0AC0000–0ACFFFF |
| SA173 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 128/64 | 15A0000–15BFFFF | 0AD0000–0ADFFFF |
| SA174 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 128/64 | 15C0000–15DFFFF | 0AE0000–0AEFFFF |
| SA175 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 128/64 | 15E0000–15FFFFF | 0AF0000–0AFFFFF |
| SA176 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 128/64 | 1600000–161FFFF | 0B00000–0B0FFFF |
| SA177 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 128/64 | 1620000–163FFFF | 0B10000–0B1FFFF |
| SA178 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 128/64 | 1640000–165FFFFF | 0B20000–0B2FFFF |
| SA179 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 128/64 | 1660000–167FFFF | 0B30000–0B3FFFF |
| SA180 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 128/64 | 1680000–169FFFF | 0B40000–0B4FFFF |
| SA181 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 128/64 | 16A0000–16BFFFF | 0B50000–0B5FFFF |
| SA182 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 128/64 | 16C0000–16DFFFF | 0B60000–0B6FFFF |
| SA183 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 128/64 | 16E0000–16FFFFF | 0B70000–0B7FFFF |
| SA184 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 128/64 | 1700000–171FFFF | 0B80000–0B8FFFF |
| SA185 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 128/64 | 1720000–173FFFF | 0B90000–0B9FFFF |
| SA186 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 128/64 | 1740000–175FFFF | 0BA0000–0BAFFFF |
| SA187 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 128/64 | 1760000–177FFFF | 0BB0000–0BBFFFF |
| SA188 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 128/64 | 1780000–179FFFF | 0BC0000–0BCFFFF |
| SA189 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 128/64 | 17A0000–17BFFFF | 0BD0000–0BDFFFF |
| SA190 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 128/64 | 17C0000–17DFFFF | 0BE0000–0BEFFFF |
| SA191 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 128/64 | 17E0000–17FFFFF | 0BF0000–0BFFFFF |
| SA192 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 128/64 | 1800000–181FFFF | 0C00000–0C0FFFF |
| SA193 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 128/64 | 1820000–183FFFF | 0C10000–0C1FFFF |
| SA194 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 128/64 | 1840000–185FFFF | 0C20000–0C2FFFF |
| SA195 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 128/64 | 1860000–187FFFF | 0C30000–0C3FFFF |
| SA196 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 128/64 | 1880000–189FFFF | 0C40000–0C4FFFF |
| SA197 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 128/64 | 18A0000–18BFFFF | 0C50000–0C5FFFF |

**Table 2. Sector Address Table–S29GL256N (Continued)**

| Sector | A23–A16 | | | | | | | | Sector Size (Kbytes/ Kwords) | 8-bit Address Range (in hexadecimal) | 16-bit Address Range (in hexadecimal) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SA198 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 128/64 | 18C0000–18DFFFF | 0C60000–0C6FFFF |
| SA199 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 128/64 | 18E0000–18FFFFF | 0C70000–0C7FFFF |
| SA200 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 128/64 | 1900000–191FFFF | 0C80000–0C8FFFF |
| SA201 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 128/64 | 1920000–193FFFF | 0C90000–0C9FFFF |
| SA202 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 128/64 | 1940000–195FFFF | 0CA0000–0CAFFFF |
| SA203 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 128/64 | 1960000–197FFFF | 0CB0000–0CBFFFF |
| SA204 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 128/64 | 1980000–199FFFF | 0CC0000–0CCFFFF |
| SA205 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 128/64 | 19A0000–19BFFFF | 0CD0000–0CDFFFF |
| SA206 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 128/64 | 19C0000–19DFFFF | 0CE0000–0CEFFFF |
| SA207 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 128/64 | 19E0000–19FFFF | 0CF0000–0CFFFFF |
| SA208 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 128/64 | 1A00000–1A1FFFF | 0D00000–0D0FFFF |
| SA209 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 128/64 | 1A20000–1A3FFFF | 0D10000–0D1FFFF |
| SA210 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 128/64 | 1A40000–1A5FFFF | 0D20000–0D2FFFF |
| SA211 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 128/64 | 1A60000–1A7FFFF | 0D30000–0D3FFFF |
| SA212 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 128/64 | 1A80000–1A9FFFF | 0D40000–0D4FFFF |
| SA213 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 128/64 | 1AA0000–1ABFFFF | 0D50000–0D5FFFF |
| SA214 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 128/64 | 1AC0000–1ADFFFF | 0D60000–0D6FFFF |
| SA215 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 128/64 | 1AE0000–1AFFFFF | 0D70000–0D7FFFF |
| SA216 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 128/64 | 1B00000–1B1FFFF | 0D80000–0D8FFFF |
| SA217 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 128/64 | 1B20000–1B3FFFF | 0D90000–0D9FFFF |
| SA218 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 128/64 | 1B40000–1B5FFFF | 0DA0000–0DAFFFF |
| SA219 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 128/64 | 1B60000–1B7FFFF | 0DB0000–0DBFFFF |
| SA220 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 128/64 | 1B80000–1B9FFFF | 0DC0000–0DCFFFF |
| SA221 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 128/64 | 1BA0000–1BBFFFF | 0DD0000–0DDFFFF |
| SA222 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 128/64 | 1BC0000–1BDFFFF | 0DE0000–0DEFFFF |
| SA223 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 128/64 | 1BE0000–1BFFFFF | 0DF0000–0DFFFFF |
| SA224 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 128/64 | 1C00000–1C1FFFF | 0E00000–0E0FFFF |
| SA225 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 128/64 | 1C20000–1C3FFFF | 0E10000–0E1FFFF |
| SA226 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 128/64 | 1C40000–1C5FFFF | 0E20000–0E2FFFF |
| SA227 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 128/64 | 1C60000–1C7FFFF | 0E30000–0E3FFFF |
| SA228 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 128/64 | 1C80000–1C9FFFF | 0E40000–0E4FFFF |
| SA229 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 128/64 | 1CA0000–1CBFFFF | 0E50000–0E5FFFF |
| SA230 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 128/64 | 1CC0000–1CDFFFF | 0E60000–0E6FFFF |
| SA231 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 128/64 | 1CE0000–1CFFFFF | 0E70000–0E7FFFF |
| SA232 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 128/64 | 1D00000–1D1FFFF | 0E80000–0E8FFFF |

## Table 2. Sector Address Table–S29GL256N (Continued)

| Sector | A23–A16 | | | | | | | | Sector Size (Kbytes/ Kwords) | 8-bit Address Range (in hexadecimal) | 16-bit Address Range (in hexadecimal) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SA233 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 128/64 | 1D20000–1D3FFFF | 0E90000–0E9FFFF |
| SA234 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 128/64 | 1D40000–1D5FFFF | 0EA0000–0EAFFFF |
| SA235 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 128/64 | 1D60000–1D7FFFF | 0EB0000–0EBFFFF |
| SA236 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 128/64 | 1D80000–1D9FFFF | 0EC0000–0ECFFFF |
| SA237 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 128/64 | 1DA0000–1DBFFFF | 0ED0000–0EDFFFF |
| SA238 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 128/64 | 1DC0000–1DDFFFF | 0EE0000–0EEFFFF |
| SA239 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 128/64 | 1DE0000–1DFFFFF | 0EF0000–0EFFFFF |
| SA240 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 128/64 | 1E00000–1E1FFFF | 0F00000–0F0FFFF |
| SA241 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 128/64 | 1E20000–1E3FFFF | 0F10000–0F1FFFF |
| SA242 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 128/64 | 1E40000–1E5FFFF | 0F20000–0F2FFFF |
| SA243 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 128/64 | 1E60000–137FFFF | 0F30000–0F3FFFF |
| SA244 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 128/64 | 1E80000–1E9FFFF | 0F40000–0F4FFFF |
| SA245 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 128/64 | 1EA0000–1EBFFFF | 0F50000–0F5FFFF |
| SA246 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 128/64 | 1EC0000–1EDFFFF | 0F60000–0F6FFFF |
| SA247 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 128/64 | 1EE0000–1EFFFFF | 0F70000–0F7FFFF |
| SA248 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 128/64 | 1F00000–1F1FFFF | 0F80000–0F8FFFF |
| SA249 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 128/64 | 1F20000–1F3FFFF | 0F90000–0F9FFFF |
| SA250 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 128/64 | 1F40000–1F5FFFF | 0FA0000–0FAFFFF |
| SA251 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 128/64 | 1F60000–1F7FFFF | 0FB0000–0FBFFFF |
| SA252 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 128/64 | 1F80000–1F9FFFF | 0FC0000–0FCFFFF |
| SA253 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 128/64 | 1FA0000–1FBFFFF | 0FD0000–0FDFFFF |
| SA254 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 128/64 | 1FC0000–1FDFFFF | 0FE0000–0FEFFFF |
| SA255 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 128/64 | 1FE0000–1FFFFFF | 0FF0000–0FFFFFF |

## Table 3. Sector Address Table–S29GLI28N

| Sector | A22–A16 | | | | | | Sector Size (Kbytes/ Kwords) | 8-Bit Address Range (in hexadecimal) | 16-bit Address Range (in hexadecimal) |
|---|---|---|---|---|---|---|---|---|---|
| SA0 | 0 | 0 | 0 | 0 | 0 | 0 | 128/64 | 0000000–001FFFF | 0000000–000FFFF |
| SA1 | 0 | 0 | 0 | 0 | 0 | 1 | 128/64 | 0020000–003FFFF | 0010000–001FFFF |
| SA2 | 0 | 0 | 0 | 0 | 1 | 0 | 128/64 | 0040000–005FFFF | 0020000–002FFFF |
| SA3 | 0 | 0 | 0 | 0 | 1 | 1 | 128/64 | 0060000–007FFFF | 0030000–003FFFF |
| SA4 | 0 | 0 | 0 | 1 | 0 | 0 | 128/64 | 0080000–009FFFF | 0040000–004FFFF |
| SA5 | 0 | 0 | 0 | 1 | 0 | 1 | 128/64 | 00A0000–00BFFFF | 0050000–005FFFF |
| SA6 | 0 | 0 | 0 | 1 | 1 | 0 | 128/64 | 00C0000–00DFFFF | 0060000–006FFFF |

**Table 3. Sector Address Table–S29GLI28N (Continued)**

| Sector | A22–A16 | | | | | | Sector Size (Kbytes/ Kwords) | 8-Bit Address Range (in hexadecimal) | 16-bit Address Range (in hexadecimal) |
|---|---|---|---|---|---|---|---|---|---|
| SA7 | 0 | 0 | 0 | 1 | 1 | 1 | 128/64 | 00E0000–00FFFFF | 0070000–007FFFF |
| SA8 | 0 | 0 | 1 | 0 | 0 | 0 | 128/64 | 0100000–011FFFF | 0080000–008FFFF |
| SA9 | 0 | 0 | 1 | 0 | 0 | 1 | 128/64 | 0120000–013FFFF | 0090000–009FFFF |
| SA10 | 0 | 0 | 1 | 0 | 1 | 0 | 128/64 | 0140000–015FFFF | 00A0000–00AFFFF |
| SA11 | 0 | 0 | 1 | 0 | 1 | 1 | 128/64 | 0160000–017FFFF | 00B0000–00BFFFF |
| SA12 | 0 | 0 | 1 | 1 | 0 | 0 | 128/64 | 0180000–019FFFF | 00C0000–00CFFFF |
| SA13 | 0 | 0 | 1 | 1 | 0 | 1 | 128/64 | 01A0000–01BFFFF | 00D0000–00DFFFF |
| SA14 | 0 | 0 | 1 | 1 | 1 | 0 | 128/64 | 01C0000–01DFFFF | 00E0000–00EFFFF |
| SA15 | 0 | 0 | 1 | 1 | 1 | 1 | 128/64 | 01E0000–01FFFFF | 00F0000–00FFFFF |
| SA16 | 0 | 1 | 0 | 0 | 0 | 0 | 128/64 | 0200000–021FFFF | 0100000–010FFFF |
| SA17 | 0 | 1 | 0 | 0 | 0 | 1 | 128/64 | 0220000–023FFFF | 0110000–011FFFF |
| SA18 | 0 | 1 | 0 | 0 | 1 | 0 | 128/64 | 0240000–025FFFF | 0120000–012FFFF |
| SA19 | 0 | 1 | 0 | 0 | 1 | 1 | 128/64 | 0260000–027FFFF | 0130000–013FFFF |
| SA20 | 0 | 1 | 0 | 1 | 0 | 0 | 128/64 | 0280000–029FFFF | 0140000–014FFFF |
| SA21 | 0 | 1 | 0 | 1 | 0 | 1 | 128/64 | 02A0000–02BFFFF | 0150000–015FFFF |
| SA22 | 0 | 1 | 0 | 1 | 1 | 0 | 128/64 | 02C0000–02DFFFF | 0160000–016FFFF |
| SA23 | 0 | 1 | 0 | 1 | 1 | 1 | 128/64 | 02E0000–02FFFFF | 0170000–017FFFF |
| SA24 | 0 | 1 | 1 | 0 | 0 | 0 | 128/64 | 0300000–031FFFF | 0180000–018FFFF |
| SA25 | 0 | 1 | 1 | 0 | 0 | 1 | 128/64 | 0320000–033FFFF | 0190000–019FFFF |
| SA26 | 0 | 1 | 1 | 0 | 1 | 0 | 128/64 | 0340000–035FFFF | 01A0000–01AFFFF |
| SA27 | 0 | 1 | 1 | 0 | 1 | 1 | 128/64 | 0360000–037FFFF | 01B0000–01BFFFF |
| SA28 | 0 | 1 | 1 | 1 | 0 | 0 | 128/64 | 0380000–039FFFF | 01C0000–01CFFFF |
| SA29 | 0 | 1 | 1 | 1 | 0 | 1 | 128/64 | 03A0000–03BFFFF | 01D0000–01DFFFF |
| SA30 | 0 | 1 | 1 | 1 | 1 | 0 | 128/64 | 03C0000–03DFFFF | 01E0000–01EFFFF |
| SA31 | 0 | 1 | 1 | 1 | 1 | 1 | 128/64 | 03E0000–03FFFFF | 01F0000–01FFFFF |
| SA32 | 1 | 0 | 0 | 0 | 0 | 0 | 128/64 | 0400000–041FFFF | 0200000–020FFFF |
| SA33 | 1 | 0 | 0 | 0 | 0 | 1 | 128/64 | 0420000–043FFFF | 0210000–021FFFF |
| SA34 | 1 | 0 | 0 | 0 | 1 | 0 | 128/64 | 0440000–045FFFF | 0220000–022FFFF |
| SA35 | 1 | 0 | 0 | 0 | 1 | 1 | 128/64 | 0460000–047FFFF | 0230000–023FFFF |
| SA36 | 1 | 0 | 0 | 1 | 0 | 0 | 128/64 | 0480000–049FFFF | 0240000–024FFFF |
| SA37 | 1 | 0 | 0 | 1 | 0 | 1 | 128/64 | 04A0000–04BFFFF | 0250000–025FFFF |
| SA38 | 1 | 0 | 0 | 1 | 1 | 0 | 128/64 | 04C0000–04DFFFF | 0260000–026FFFF |
| SA39 | 1 | 0 | 0 | 1 | 1 | 1 | 128/64 | 04E0000–04FFFFF | 0270000–027FFFF |
| SA40 | 1 | 0 | 1 | 0 | 0 | 0 | 128/64 | 0500000–051FFFF | 0280000–028FFFF |
| SA41 | 1 | 0 | 1 | 0 | 0 | 1 | 128/64 | 0520000–053FFFF | 0290000–029FFFF |

## Table 3. Sector Address Table–S29GLI28N (Continued)

| Sector | A22–A16 | | | | | | Sector Size (Kbytes/ Kwords) | 8-Bit Address Range (in hexadecimal) | 16-bit Address Range (in hexadecimal) |
|---|---|---|---|---|---|---|---|---|---|
| SA42 | 1 | 0 | 1 | 0 | 1 | 0 | 128/64 | 0540000–055FFFF | 02A0000–02AFFFF |
| SA43 | 1 | 0 | 1 | 0 | 1 | 1 | 128/64 | 0560000–057FFFF | 02B0000–02BFFFF |
| SA44 | 1 | 0 | 1 | 1 | 0 | 0 | 128/64 | 0580000–059FFFF | 02C0000–02CFFFF |
| SA45 | 1 | 0 | 1 | 1 | 0 | 1 | 128/64 | 05A0000–05BFFFF | 02D0000–02DFFFF |
| SA46 | 1 | 0 | 1 | 1 | 1 | 0 | 128/64 | 05C0000–05DFFFF | 02E0000–02EFFFF |
| SA47 | 1 | 0 | 1 | 1 | 1 | 1 | 128/64 | 05E0000–05FFFFF | 02F0000–02FFFFF |
| SA48 | 1 | 1 | 0 | 0 | 0 | 0 | 128/64 | 0600000–061FFFF | 0300000–030FFFF |
| SA49 | 1 | 1 | 0 | 0 | 0 | 1 | 128/64 | 0620000–063FFFF | 0310000–031FFFF |
| SA50 | 1 | 1 | 0 | 0 | 1 | 0 | 128/64 | 0640000–065FFFF | 0320000–032FFFF |
| SA51 | 1 | 1 | 0 | 0 | 1 | 1 | 128/64 | 0660000–067FFFF | 0330000–033FFFF |
| SA52 | 1 | 1 | 0 | 1 | 0 | 0 | 128/64 | 0680000–069FFFF | 0340000–034FFFF |
| SA53 | 1 | 1 | 0 | 1 | 0 | 1 | 128/64 | 06A0000–06BFFFF | 0350000–035FFFF |
| SA54 | 1 | 1 | 0 | 1 | 1 | 0 | 128/64 | 06C0000–06DFFFF | 0360000–036FFFF |
| SA55 | 1 | 1 | 0 | 1 | 1 | 1 | 128/64 | 06E0000–06FFFFF | 0370000–037FFFF |
| SA56 | 1 | 1 | 1 | 0 | 0 | 0 | 128/64 | 0700000–071FFFF | 0380000–038FFFF |
| SA57 | 1 | 1 | 1 | 0 | 0 | 1 | 128/64 | 0720000–073FFFF | 0390000–039FFFF |
| SA58 | 1 | 1 | 1 | 0 | 1 | 0 | 128/64 | 0740000–075FFFF | 03A0000–03AFFFF |
| SA59 | 1 | 1 | 1 | 0 | 1 | 1 | 128/64 | 0760000–077FFFF | 03B0000–03BFFFF |
| SA60 | 1 | 1 | 1 | 1 | 0 | 0 | 128/64 | 0780000–079FFFF | 03C0000–03CFFFF |
| SA61 | 1 | 1 | 1 | 1 | 0 | 1 | 128/64 | 07A0000–07BFFFF | 03D0000–03DFFFF |
| SA62 | 1 | 1 | 1 | 1 | 1 | 0 | 128/64 | 07C0000–07DFFFF | 03E0000–03EFFFF |
| SA63 | 1 | 1 | 1 | 1 | 1 | 1 | 128/64 | 07E0000–07FFFFF | 03F0000–03FFFFF |
| SA64 | 0 | 0 | 0 | 0 | 0 | 0 | 128/64 | 0800000–081FFFF | 0400000–040FFFF |
| SA65 | 0 | 0 | 0 | 0 | 0 | 1 | 128/64 | 0820000–083FFFF | 0410000–041FFFF |
| SA66 | 0 | 0 | 0 | 0 | 1 | 0 | 128/64 | 0840000–085FFFF | 0420000–042FFFF |
| SA67 | 0 | 0 | 0 | 0 | 1 | 1 | 128/64 | 0860000–087FFFF | 0430000–043FFFF |
| SA68 | 0 | 0 | 0 | 1 | 0 | 0 | 128/64 | 0880000–089FFFF | 0440000–044FFFF |
| SA69 | 0 | 0 | 0 | 1 | 0 | 1 | 128/64 | 08A0000–08BFFFF | 0450000–045FFFF |
| SA70 | 0 | 0 | 0 | 1 | 1 | 0 | 128/64 | 08C0000–08DFFFF | 0460000–046FFFF |
| SA71 | 0 | 0 | 0 | 1 | 1 | 1 | 128/64 | 08E0000–08FFFFF | 0470000–047FFFF |
| SA72 | 0 | 0 | 1 | 0 | 0 | 0 | 128/64 | 0900000–091FFFF | 0480000–048FFFF |
| SA73 | 0 | 0 | 1 | 0 | 0 | 1 | 128/64 | 0920000–093FFFF | 0490000–049FFFF |
| SA74 | 0 | 0 | 1 | 0 | 1 | 0 | 128/64 | 0940000–095FFFF | 04A0000–04AFFFF |
| SA75 | 0 | 0 | 1 | 0 | 1 | 1 | 128/64 | 0960000–097FFFF | 04B0000–04BFFFF |
| SA76 | 0 | 0 | 1 | 1 | 0 | 0 | 128/64 | 0980000–099FFFF | 04C0000–04CFFFF |

**Table 3. Sector Address Table–S29GLI28N (Continued)**

| Sector | A22–A16 | | | | | | Sector Size (Kbytes/ Kwords) | 8-Bit Address Range (in hexadecimal) | 16-bit Address Range (in hexadecimal) |
|---|---|---|---|---|---|---|---|---|---|
| SA77 | 0 | 0 | 1 | 1 | 0 | 1 | 128/64 | 09A0000–09BFFFF | 04D0000–04DFFFF |
| SA78 | 0 | 0 | 1 | 1 | 1 | 0 | 128/64 | 09C0000–09DFFFF | 04E0000–04EFFFF |
| SA79 | 0 | 0 | 1 | 1 | 1 | 1 | 128/64 | 09E0000–09FFFFF | 04F0000–04FFFFF |
| SA80 | 0 | 1 | 0 | 0 | 0 | 0 | 128/64 | 0A00000–0A1FFFF | 0500000–050FFFF |
| SA81 | 0 | 1 | 0 | 0 | 0 | 1 | 128/64 | 0A20000–0A3FFFF | 0510000–051FFFF |
| SA82 | 0 | 1 | 0 | 0 | 1 | 0 | 128/64 | 0A40000–0A5FFFF | 0520000–052FFFF |
| SA83 | 0 | 1 | 0 | 0 | 1 | 1 | 128/64 | 0A60000–0A7FFFF | 0530000–053FFFF |
| SA84 | 0 | 1 | 0 | 1 | 0 | 0 | 128/64 | 0A80000–0A9FFFF | 0540000–054FFFF |
| SA85 | 0 | 1 | 0 | 1 | 0 | 1 | 128/64 | 0AA0000–0ABFFFF | 0550000–055FFFF |
| SA86 | 0 | 1 | 0 | 1 | 1 | 0 | 128/64 | 0AC0000–0ADFFFF | 0560000–056FFFF |
| SA87 | 0 | 1 | 0 | 1 | 1 | 1 | 128/64 | 0AE0000–0AFFFFF | 0570000–057FFFF |
| SA88 | 0 | 1 | 1 | 0 | 0 | 0 | 128/64 | 0B00000–0B1FFFF | 0580000–058FFFF |
| SA89 | 0 | 1 | 1 | 0 | 0 | 1 | 128/64 | 0B20000–0B3FFFF | 0590000–059FFFF |
| SA90 | 0 | 1 | 1 | 0 | 1 | 0 | 128/64 | 0B40000–0B5FFFF | 05A0000–05AFFFF |
| SA91 | 0 | 1 | 1 | 0 | 1 | 1 | 128/64 | 0B60000–0B7FFFF | 05B0000–05BFFFF |
| SA92 | 0 | 1 | 1 | 1 | 0 | 0 | 128/64 | 0B80000–0B9FFFF | 05C0000–05CFFFF |
| SA93 | 0 | 1 | 1 | 1 | 0 | 1 | 128/64 | 0BA0000–0BBFFFF | 05D0000–05DFFFF |
| SA94 | 0 | 1 | 1 | 1 | 1 | 0 | 128/64 | 0BC0000–0BDFFFF | 05E0000–05EFFFF |
| SA95 | 0 | 1 | 1 | 1 | 1 | 1 | 128/64 | 0BE0000–0BFFFFF | 05F0000–05FFFFF |
| SA96 | 1 | 0 | 0 | 0 | 0 | 0 | 128/64 | 0C00000–0C1FFFF | 0600000–060FFFF |
| SA97 | 1 | 0 | 0 | 0 | 0 | 1 | 128/64 | 0C20000–0C3FFFF | 0610000–061FFFF |
| SA98 | 1 | 0 | 0 | 0 | 1 | 0 | 128/64 | 0C40000–0C5FFFF | 0620000–062FFFF |
| SA99 | 1 | 0 | 0 | 0 | 1 | 1 | 128/64 | 0C60000–0C7FFFF | 0630000–063FFFF |
| SA100 | 1 | 0 | 0 | 1 | 0 | 0 | 128/64 | 0C80000–0C9FFFF | 0640000–064FFFF |
| SA101 | 1 | 0 | 0 | 1 | 0 | 1 | 128/64 | 0CA0000–0CBFFFF | 0650000–065FFFF |
| SA102 | 1 | 0 | 0 | 1 | 1 | 0 | 128/64 | 0CC0000–0CDFFFF | 0660000–066FFFF |
| SA103 | 1 | 0 | 0 | 1 | 1 | 1 | 128/64 | 0CE0000–0CFFFFF | 0670000–067FFFF |
| SA104 | 1 | 0 | 1 | 0 | 0 | 0 | 128/64 | 0D00000–0D1FFFF | 0680000–068FFFF |
| SA105 | 1 | 0 | 1 | 0 | 0 | 1 | 128/64 | 0D20000–0D3FFFF | 0690000–069FFFF |
| SA106 | 1 | 0 | 1 | 0 | 1 | 0 | 128/64 | 0D40000–0D5FFFF | 06A0000–06AFFFF |
| SA107 | 1 | 0 | 1 | 0 | 1 | 1 | 128/64 | 0D60000–0D7FFFF | 06B0000–06BFFFF |
| SA108 | 1 | 0 | 1 | 1 | 0 | 0 | 128/64 | 0D80000–0D9FFFF | 06C0000–06CFFFF |
| SA109 | 1 | 0 | 1 | 1 | 0 | 1 | 128/64 | 0DA0000–0DBFFFF | 06D0000–06DFFFF |
| SA110 | 1 | 0 | 1 | 1 | 1 | 0 | 128/64 | 0DC0000–0DDFFFF | 06E0000–06EFFFF |
| SA111 | 1 | 0 | 1 | 1 | 1 | 1 | 128/64 | 0DE0000–0DFFFFF | 06F0000–06FFFFF |

**Table 3. Sector Address Table–S29GLI28N (Continued)**

| Sector | A22–A16 | | | | | | Sector Size (Kbytes/ Kwords) | 8-Bit Address Range (in hexadecimal) | 16-bit Address Range (in hexadecimal) |
|---|---|---|---|---|---|---|---|---|---|
| SA112 | 1 | 1 | 0 | 0 | 0 | 0 | 128/64 | 0E00000–0E1FFFF | 0700000–070FFFF |
| SA113 | 1 | 1 | 0 | 0 | 0 | 1 | 128/64 | 0E20000–0E3FFFF | 0710000–071FFFF |
| SA114 | 1 | 1 | 0 | 0 | 1 | 0 | 128/64 | 0E40000–0E5FFFF | 0720000–072FFFF |
| SA115 | 1 | 1 | 0 | 0 | 1 | 1 | 128/64 | 0E60000–0E7FFFF | 0730000–073FFFF |
| SA116 | 1 | 1 | 0 | 1 | 0 | 0 | 128/64 | 0E80000–0E9FFFF | 0740000–074FFFF |
| SA117 | 1 | 1 | 0 | 1 | 0 | 1 | 128/64 | 0EA0000–0EBFFFF | 0750000–075FFFF |
| SA118 | 1 | 1 | 0 | 1 | 1 | 0 | 128/64 | 0EC0000–0EDFFFF | 0760000–076FFFF |
| SA119 | 1 | 1 | 0 | 1 | 1 | 1 | 128/64 | 0EE0000–0EFFFFF | 0770000–077FFFF |
| SA120 | 1 | 1 | 1 | 0 | 0 | 0 | 128/64 | 0F00000–0F1FFFF | 0780000–078FFFF |
| SA121 | 1 | 1 | 1 | 0 | 0 | 1 | 128/64 | 0F20000–0F3FFFF | 0790000–079FFFF |
| SA122 | 1 | 1 | 1 | 0 | 1 | 0 | 128/64 | 0F40000–0F5FFFF | 07A0000–07AFFFF |
| SA123 | 1 | 1 | 1 | 0 | 1 | 1 | 128/64 | 0F60000–0F7FFFF | 07B0000–07BFFFF |
| SA124 | 1 | 1 | 1 | 1 | 0 | 0 | 128/64 | 0F80000–0F9FFFF | 07C0000–07CFFFF |
| SA125 | 1 | 1 | 1 | 1 | 0 | 1 | 128/64 | 0FA0000–0FBFFFF | 07D0000–07DFFFF |
| SA126 | 1 | 1 | 1 | 1 | 1 | 0 | 128/64 | 0FC0000–0FDFFFF | 07E0000–07EFFFF |
| SA127 | 1 | 1 | 1 | 1 | 1 | 1 | 128/64 | 0FE0000–0FFFFFF | 07F0000–07FFFFF |

## Sector Protection

The device features several levels of sector protection, which can disable both the program and erase operations in certain sectors or sector groups:

### *Persistent Sector Protection*

A command sector protection method that replaces the old 12 V controlled protection method.

### *Password Sector Protection*

A highly sophisticated protection method that requires a password before changes to certain sectors or sector groups are permitted

### *WP# Hardware Protection*

A write protect pin that can prevent program or erase operations in the outermost sectors.

The WP# Hardware Protection feature is always available, independent of the software managed protection method chosen.

### Selecting a Sector Protection Mode

All parts default to operate in the Persistent Sector Protection mode. The customer must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which sector protection method will be used. If the customer decides to continue using the Persistent Sector Protection method, they must set the **Persistent Sector Protection Mode Locking Bit**. This will permanently set the part to op-

erate only using Persistent Sector Protection. If the customer decides to use the password method, they must set the **Password Mode Locking Bit**. This will permanently set the part to operate only using password sector protection.

It is important to remember that setting either the **Persistent Sector Protection Mode Locking Bit** or the **Password Mode Locking Bit** permanently selects the protection mode. It is not possible to switch between the two methods once a locking bit has been set. **It is important that one mode is explicitly selected when the device is first programmed, rather than relying on the default mode alone.** This is so that it is not possible for a system program or virus to later set the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Protection Mode.

The device is shipped with all sectors unprotected. The factory offers the option of programming and protecting sectors at the factory prior to shipping the device through the ExpressFlash™ Service. Contact your sales representative for details.

It is possible to determine whether a sector is protected or unprotected. See "Autoselect Command Sequence" section on page 50 for details.

## Advanced Sector Protection

Advanced Sector Protection features several levels of sector protection, which can disable both the program and erase operations in certain sectors.

**Persistent Sector Protection** is a method that replaces the old 12V controlled protection method.

**Password Sector Protection** is a highly sophisticated protection method that requires a password before changes to certain sectors are permitted.

Advanced Sector Protection is available when ACC = $V_{HH}$.

## Lock Register

The Lock Register consists of 3 bits (DQ2, DQ1, and DQ0). These DQ2, DQ1, DQ0 bits of the Lock Register are programmable by the user. Users are not allowed to program both DQ2 and DQ1 bits of the Lock Register to the 00 state. If the user tries to program DQ2 and DQ1 bits of the Lock Register to the 00 state, the device will abort the Lock Register back to the default 11 state. The programming time of the Lock Register is same as the typical word programming time without utilizing the Write Buffer of the device. During a Lock Register programming sequence execution, the DQ6 Toggle Bit I will toggle until the programming of the Lock Register has completed to indicate programming status. All Lock Register bits are readable to allow users to verify Lock Register statuses. Initial access delay is required to read the Lock Register.

The Customer Secured Silicon Sector Protection Bit is DQ0, Persistent Protection Mode Lock Bit is DQ1, and Password Protection Mode Lock Bit is DQ2 are accessible by all users. Each of these bits are non-volatile. DQ15-DQ3 are reserved and must be 1's when the user tries to program the DQ2, DQ1, and DQ0 bits of the Lock Register. The user is not required to program DQ2, DQ1 and DQ0 bits of the Lock Register at the same time. This allows users to lock the Secured Silicon Sector and then set the device either permanently into Password Protection Mode or Persistent Protection Mode and then lock the Secured Silicon Sector at separate instances and time frames.

- Secured Silicon Sector Protection allows the user to lock the Secured Silicon Sector area

- Persistent Protection Mode Lock Bit allows the user to set the device permanently to operate in the Persistent Protection Mode
- Password Protection Mode Lock Bit allows the user to set the device permanently to operate in the Password Protection Mode

**Table 4. Lock Register**

| DQ15-3 | DQ2 | DQ1 | DQ0 |
|---|---|---|---|
| Don't Care | Password Protection Mode Lock Bit | Persistent Protection Mode Lock Bit | Secured Silicon Sector Protection Bit |

## Persistent Sector Protection

The Persistent Sector Protection method replaces the old 12 V controlled protection method while at the same time enhancing flexibility by providing three different sector protection states:

- **Dynamically Locked**-The sector is protected and can be changed by a simple command
- **Persistently Locked**-A sector is protected and cannot be changed
- **Unlocked**-The sector is unprotected and can be changed by a simple command

In order to achieve these states, three types of "bits" are going to be used:

### Dynamic Protection Bit (DYB)

A volatile protection bit is assigned for each sector. After power-up or hardware reset, the contents of all DYB bits are in the "unprotected state" if the DYB Lock Bit of the "Lock Register" is not programmed. If the DYB Lock Bit of the "Lock Register" is programmed, all DYB bits will power-up or hardware reset to the "protected state". Each DYB is individually modifiable through the DYB Set Command and DYB Clear Command. When the parts are first shipped, all of the Persistent Protect Bits (PPB) are cleared into the unprotected state. The DYB bits and PPB Lock bit are defaulted to power up in the cleared state or unprotected state - meaning the all PPB bits are changeable.

The Protection State for each sector is determined by the logical OR of the PPB and the DYB related to that sector. For the sectors that have the PPB bits cleared, the DYB bits control whether or not the sector is protected or unprotected. By issuing the DYB Set and DYB Clear command sequences, the DYB bits will be protected or unprotected, thus placing each sector in the protected or unprotected state. These are the so-called Dynamic Locked or Unlocked states. They are called dynamic states because it is very easy to switch back and forth between the protected and un-protected conditions. This allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed.

The DYB bits maybe set or cleared as often as needed. The PPB bits allow for a more static, and difficult to change, level of protection. The PPB bits retain their state across power cycles because they are Non-Volatile. Individual PPB bits are set with a program command but must all be cleared as a group through an erase command.

The PPB Lock Bit adds an additional level of protection. Once all PPB bits are programmed to the desired settings, the PPB Lock Bit may be set to the "freeze

state". Setting the PPB Lock Bit to the "freeze state" disables all program and erase commands to the Non-Volatile PPB bits. In effect, the PPB Lock Bit locks the PPB bits into their current state. The only way to clear the PPB Lock Bit to the "unfreeze state" is to go through a power cycle, or hardware reset. The Software Reset command will not clear the PPB Lock Bit to the "unfreeze state". System boot code can determine if any changes to the PPB bits are needed e.g. to allow new system code to be downloaded. If no changes are needed then the boot code can set the PPB Lock Bit to disable any further changes to the PPB bits during system operation.

The WP# write protect pin adds a final level of hardware protection. When this pin is low it is not possible to change the contents of the WP# protected sectors. These sectors generally hold system boot code. So, the WP# pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DYB Set command sequence is all that is necessary. The DYB Set and DYB Clear commands for the dynamic sectors switch the DYB bits to signify protected and unprotected, respectively. If there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock Bit must be disabled to the "unfreeze state" by either putting the device through a power-cycle, or hardware reset. The PPB bits can then be changed to reflect the desired settings. Setting the PPB Lock Bit once again to the "freeze state" will lock the PPB bits, and the device operates normally again.

Note: to achieve the best protection, it's recommended to execute the PPB Lock Bit Set command early in the boot code, and protect the boot code by holding WP# = $V_{IL}$.

### Persistent Protection Bit (PPB)

A single Persistent (non-volatile) Protection Bit is assigned to each sector. If a PPB is programmed to the protected state through the "PPB Program" command, that sector will be protected from program or erase operations will be read-only. If a PPB requires erasure, all of the sector PPB bits must first be erased in parallel through the "All PPB Erase" command. The "All PPB Erase" command will preprogrammed all PPB bits prior to PPB erasing. All PPB bits erase in parallel, unlike programming where individual PPB bits are programmable. The PPB bits have the same endurance as the flash memory.

Programming the PPB bit requires the typical word programming time without utilizing the Write Buffer. During a PPB bit programming and A11 PPB bit erasing sequence execution, the DQ6 Toggle Bit I will toggle until the programming of the PPB bit or erasing of all PPB bits has completed to indicate programming and erasing status. Erasing all of the PPB bits at once requires typical sector erase time. During the erasing of all PPB bits, the DQ3 Sector Erase Timer bit will output a 1 to indicate the erasure of all PPB bits are in progress. When the erasure of all PPB bits has completed, the DQ3 Sector Erase Timer bit will output a 0 to indicate that all PPB bits have been erased. Reading the PPB Status bit requires the initial access time of the device.

### Persistent Protection Bit Lock (PPB Lock Bit)

A global volatile bit. When set to the "freeze state", the PPB bits cannot be changed. When cleared to the "unfreeze state", the PPB bits are changeable. There is only one PPB Lock Bit per device. The PPB Lock Bit is cleared to the "unfreeze state" after power-up or hardware reset. There is no command sequence to unlock or "unfreeze" the PPB Lock Bit.

Configuring the PPB Lock Bit to the freeze state requires approximately 100ns. Reading the PPB Lock Status bit requires the initial access time of the device.

**Table 5. Sector Protection Schemes**

| Protection States | | | Sector State |
|---|---|---|---|
| DYB Bit | PPB Bit | PPB Lock Bit | |
| Unprotect | Unprotect | Unfreeze | Unprotected – PPB and DYB are changeable |
| Unprotect | Unprotect | Freeze | Unprotected – PPB not changeable, DYB is changeable |
| Unprotect | Protect | Unfreeze | Protected – PPB and DYB are changeable |
| Unprotect | Protect | Freeze | Protected – PPB not changeable, DYB is changeable |
| Protect | Unprotect | Unfreeze | Protected – PPB and DYB are changeable |
| Protect | Unprotect | Freeze | Protected – PPB not changeable, DYB is changeable |
| Protect | Protect | Unfreeze | Protected – PPB and DYB are changeable |
| Protect | Protect | Freeze | Protected – PPB not changeable, DYB is changeable |

Table 7 contains all possible combinations of the DYB bit, PPB bit, and PPB Lock Bit relating to the status of the sector. In summary, if the PPB bit is set, and the PPB Lock Bit is set, the sector is protected and the protection cannot be removed until the next power cycle or hardware reset clears the PPB Lock Bit to "unfreeze state". If the PPB bit is cleared, the sector can be dynamically locked or unlocked. The DYB bit then controls whether or not the sector is protected or unprotected. If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program command to a protected sector enables status polling for approximately 1 µs before the device returns to read mode without having modified the contents of the protected sector. An erase command to a protected sector enables status polling for approximately 50 µs after which the device returns to read mode without having erased the protected sector. The programming of the DYB bit, PPB bit, and PPB Lock Bit for a given sector can be verified by writing a DYB Status Read, PPB Status Read, and PPB Lock Status Read commands to the device.

The Autoselect Sector Protection Verification outputs the OR function of the DYB bit and PPB bit per sector basis. When the OR function of the DYB bit and PPB bit is a 1, the sector is either protected by DYB or PPB or both. When the OR function of the DYB bit and PPB bit is a 0, the sector is unprotected through both the DYB and PPB.

## Persistent Protection Mode Lock Bit

Like the Password Protection Mode Lock Bit, a Persistent Protection Mode Lock Bit exists to guarantee that the device remain in software sector protection. Once programmed, the Persistent Protection Mode Lock Bit prevents programming of

the Password Protection Mode Lock Bit. This guarantees that a hacker could not place the device in Password Protection Mode. The Password Protection Mode Lock Bit resides in the "Lock Register".

## Password Sector Protection

The Password Sector Protection method allows an even higher level of security than the Persistent Sector Protection method. There are two main differences between the Persistent Sector Protection and the Password Sector Protection methods:

- When the device is first powered on, or comes out of a reset cycle, the PPB Lock Bit is set to the locked state, or the freeze state, rather than cleared to the unlocked state, or the unfreeze state.
- The only means to clear and unfreeze the PPB Lock Bit is by writing a unique 64-bit Password to the device.

The Password Sector Protection method is otherwise identical to the Persistent Sector Protection method.

A 64-bit password is the only additional tool utilized in this method.

The password is stored in a one-time programmable (OTP) region outside of the flash memory. Once the Password Protection Mode Lock Bit is set, the password is permanently set with no means to read, program, or erase it. The password is used to clear and unfreeze the PPB Lock Bit. The Password Unlock command must be written to the flash, along with a password. The flash device internally compares the given password with the pre-programmed password. If they match, the PPB Lock Bit is cleared to the "unfreezed state", and the PPB bits can be altered. If they do not match, the flash device does nothing. There is a built-in 2 µs delay for each "password check" after the valid 64-bit password has been entered for the PPB Lock Bit to be cleared to the "unfreezed state". This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password.

## Password and Password Protection Mode Lock Bit

In order to select the Password Sector Protection method, the customer must first program the password. The factory recommends that the password be somehow correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Read operations. Once the desired password is programmed in, the customer must then set the Password Protection Mode Lock Bit. This operation achieves two objectives:

1. It permanently sets the device to operate using the Password Protection Mode. It is not possible to reverse this function.
2. It also disables all further commands to the password region. All program, and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Sector Protection method is desired when programming the Password Protection Mode Lock Bit. More importantly, the user must be sure that the password is correct when the Password Protection Mode Lock Bit is programmed. Due to the fact that read operations are disabled, there is no means to read what the password is afterwards. If the password is lost after programming the Password Protection Mode

Lock Bit, there will be no way to clear and unfreeze the PPB Lock Bit. The Password Protection Mode Lock Bit, once programmed, prevents reading the 64-bit password on the DQ bus and further password programming. The Password Protection Mode Lock Bit is not erasable. Once Password Protection Mode Lock Bit is programmed, the Persistent Protection Mode Lock Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

## 64-bit Password

The 64-bit Password is located in its own memory space and is accessible through the use of the Password Program and Password Read commands. The password function works in conjunction with the Password Protection Mode Lock Bit, which when programmed, prevents the Password Read command from reading the contents of the password on the pins of the device.

## Persistent Protection Bit Lock (PPB Lock Bit)

A global volatile bit. The PPB Lock Bit is a volatile bit that reflects the state of the Password Protection Mode Lock Bit after power-up reset. If the Password Protection Mode Lock Bit is also programmed after programming the Password, the Password Unlock command must be issued to clear and unfreeze the PPB Lock Bit after a hardware reset (RESET# asserted) or a power-up reset. Successful execution of the Password Unlock command clears and unfreezes the PPB Lock Bit, allowing for sector PPB bits to be modified. Without issuing the Password Unlock command, while asserting RESET#, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit to a the "freeze state".

If the Password Protection Mode Lock Bit is not programmed, the device defaults to Persistent Protection Mode. In the Persistent Protection Mode, the PPB Lock Bit is cleared to the "unfreeze state" after power-up or hardware reset. The PPB Lock Bit is set to the "freeze state" by issuing the PPB Lock Bit Set command. Once set to the "freeze state" the only means for clearing the PPB Lock Bit to the "unfreeze state" is by issuing a hardware or power-up reset. The Password Unlock command is ignored in Persistent Protection Mode.

Reading the PPB Lock Bit requires a 200ns access time.

## Secured Silicon Sector Flash Memory Region

The Secured Silicon Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The Secured Silicon Sector is 256 bytes in length, and uses a Secured Silicon Sector Indicator Bit (DQ7) to indicate whether or not the Secured Silicon Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

The factory offers the device with the Secured Silicon Sector either customer lockable (standard shipping option) or factory locked (contact an AMD sales representative for ordering information). The customer-lockable version is shipped with the Secured Silicon Sector unprotected, allowing customers to program the sector after receiving the device. The customer-lockable version also has the Secured Silicon Sector Indicator Bit permanently set to a "0." The factory-locked version is always protected when shipped from the factory, and has the Secured Silicon Sector Indicator Bit permanently set to a "1." Thus, the Secured Silicon Sector Indicator Bit prevents customer-lockable devices from being used to re-

place devices that are factory locked. *Note that the ACC function and unlock bypass modes are not available when the Secured Silicon Sector is enabled.*

The Secured Silicon sector address space in this device is allocated as follows:

| Secured Silicon Sector Address Range | Customer Lockable | ESN Factory Locked | ExpressFlash Factory Locked |
|---|---|---|---|
| 000000h–000007h | Determined by customer | ESN | ESN or determined by customer |
| 000008h–00007Fh | | Unavailable | Determined by customer |

The system accesses the Secured Silicon Sector through a command sequence (see "Write Protect (WP#)"). After the system has written the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the addresses normally occupied by the first sector (SA0). This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to sector SA0.

### Customer Lockable: Secured Silicon Sector NOT Programmed or Protected At the Factory

Unless otherwise specified, the device is shipped such that the customer may program and protect the 256-byte Secured Silicon sector.

The system may program the Secured Silicon Sector using the write-buffer, accelerated and/or unlock bypass methods, in addition to the standard programming command sequence. See Command Definitions.

Programming and protecting the Secured Silicon Sector must be used with caution since, once protected, there is no procedure available for unprotecting the Secured Silicon Sector area and none of the bits in the Secured Silicon Sector memory space can be modified in any way.

The Secured Silicon Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter Secured Silicon Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 2, except that *RESET# may be at either $V_{IH}$ or $V_{ID}$*. This allows in-system protection of the Secured Silicon Sector without raising any device pin to a high voltage. Note that this method is only applicable to the Secured Silicon Sector.
- To verify the protect/unprotect status of the Secured Silicon Sector, follow the algorithm shown in Figure 1.

Once the Secured Silicon Sector is programmed, locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return to reading and writing within the remainder of the array.

### Factory Locked: Secured Silicon Sector Programmed and Protected At the Factory

In devices with an ESN, the Secured Silicon Sector is protected when the device is shipped from the factory. The Secured Silicon Sector cannot be modified in any way. An ESN Factory Locked device has an 16-byte random ESN at addresses 000000h–000007h. Please contact your sales representative for details on ordering ESN Factory Locked devices.

Customers may opt to have their code programmed by the factory through the ExpressFlash service (Express Flash Factory Locked). The devices are then

shipped from the factory with the Secured Silicon Sector permanently locked. Contact your sales representative for details on using the ExpressFlash service.

### Write Protect (WP#)

The Write Protect function provides a hardware method of protecting the first or last sector group without using $V_{ID}$. Write Protect is one of two functions provided by the WP#/ACC input.

If the system asserts $V_{IL}$ on the WP#/ACC pin, the device disables program and erase functions in the first or last sector group independently of whether those sector groups were protected or unprotected using the method described in"Advanced Sector Protection" section on page 38. Note that if WP#/ACC is at $V_{IL}$ when the device is in the standby mode, the maximum input load current is increased. See the table in "DC Characteristics" section on page 78.

**If the system asserts $V_{IH}$ on the WP#/ACC pin, the device reverts to whether the first or last sector was previously set to be protected or unprotected using the method described in "Sector Group Protection and Unprotection". *Note that WP# has an internal pullup; when unconnected, WP# is at $V_{IH}$.***

### Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Tables 16 and 17 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during $V_{CC}$ power-up and power-down transitions, or from system noise.

#### Low $V_{CC}$ Write Inhibit

When $V_{CC}$ is less than $V_{LKO}$, the device does not accept any write cycles. This protects data during $V_{CC}$ power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until $V_{CC}$ is greater than $V_{LKO}$. The system must provide the proper signals to the control pins to prevent unintentional writes when $V_{CC}$ is greater than $V_{LKO}$.

#### Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

#### Logical Inhibit

Write cycles are inhibited by holding any one of OE# = $V_{IL}$, CE# = $V_{IH}$ or WE# = $V_{IH}$. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

#### Power-Up Write Inhibit

If WE# = CE# = $V_{IL}$ and OE# = $V_{IH}$ during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

## Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 8-11. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 8–11. The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/flash/cfi. Alternatively, contact your sales representative for copies of these documents.

**Table 6. CFI Query Identification String**

| Addresses (x16) | Data | Description |
|---|---|---|
| 10h<br>11h<br>12h | 0051h<br>0052h<br>0059h | Query Unique ASCII string "QRY" |
| 13h<br>14h | 0002h<br>0000h | Primary OEM Command Set |
| 15h<br>16h | 0040h<br>0000h | Address for Primary Extended Table |
| 17h<br>18h | 0000h<br>0000h | Alternate OEM Command Set (00h = none exists) |
| 19h<br>1Ah | 0000h<br>0000h | Address for Alternate OEM Extended Table (00h = none exists) |

**Table 7. System Interface String**

| Addresses (x16) | Data | Description |
|---|---|---|
| 1Bh | 0027h | $V_{CC}$ Min. (write/erase)<br>D7–D4: volt, D3–D0: 100 millivolt |
| 1Ch | 0036h | $V_{CC}$ Max. (write/erase)<br>D7–D4: volt, D3–D0: 100 millivolt |
| 1Dh | 0000h | $V_{PP}$ Min. voltage (00h = no $V_{PP}$ pin present) |
| 1Eh | 0000h | $V_{PP}$ Max. voltage (00h = no $V_{PP}$ pin present) |
| 1Fh | 0007h | Typical timeout per single byte/word write $2^N$ µs |
| 20h | 0007h | Typical timeout for Min. size buffer write $2^N$ µs (00h = not supported) |
| 21h | 000Ah | Typical timeout per individual block erase $2^N$ ms |
| 22h | 0000h | Typical timeout for full chip erase $2^N$ ms (00h = not supported) |
| 23h | 0001h | Max. timeout for byte/word write $2^N$ times typical |
| 24h | 0005h | Max. timeout for buffer write $2^N$ times typical |
| 25h | 0004h | Max. timeout per individual block erase $2^N$ times typical |
| 26h | 0000h | Max. timeout for full chip erase $2^N$ times typical (00h = not supported) |

**Table 8. Device Geometry Definition**

| Addresses (x16) | Data | Description |
|---|---|---|
| 27h | 001Ah<br>0019h<br>0018h | Device Size = $2^N$ byte<br>1A = 512 Mb, 19 = 256 Mb, 18 = 128 Mb |
| 28h<br>29h | 0002h<br>0000h | Flash Device Interface description (refer to CFI publication 100) |
| 2Ah<br>2Bh | 0005h<br>0000h | Max. number of byte in multi-byte write = $2^N$<br>(00h = not supported) |
| 2Ch | 0001h | Number of Erase Block Regions within device (01h = uniform device, 02h = boot device) |
| 2Dh<br>2Eh<br>2Fh<br>30h | 00xxh<br>000xh<br>0000h<br>000xh | Erase Block Region 1 Information<br>(refer to the CFI specification or CFI publication 100)<br>00FFh, 001h, 0000h, 0002h = 512 Mb<br>00FFh, 0000h, 0000h, 0002h = 256 Mb<br>007Fh, 0000h, 0000h, 0002h = 128 Mb |
| 31h<br>32h<br>33h<br>34h | 0000h<br>0000h<br>0000h<br>0000h | Erase Block Region 2 Information (refer to CFI publication 100) |
| 35h<br>36h<br>37h<br>38h | 0000h<br>0000h<br>0000h<br>0000h | Erase Block Region 3 Information (refer to CFI publication 100) |
| 39h<br>3Ah<br>3Bh<br>3Ch | 0000h<br>0000h<br>0000h<br>0000h | Erase Block Region 4 Information (refer to CFI publication 100) |

**Table 9. Primary Vendor-Specific Extended Query**

| Addresses (x16) | Data | Description |
|---|---|---|
| 40h<br>41h<br>42h | 0050h<br>0052h<br>0049h | Query-unique ASCII string "PRI" |
| 43h | 0031h | Major version number, ASCII |
| 44h | 0033h | Minor version number, ASCII |
| 45h | 0010h | Address Sensitive Unlock (Bits 1-0)<br>0 = Required, 1 = Not Required<br>Process Technology (Bits 7-2) 0100b = 110 nm MirrorBit |
| 46h | 0002h | Erase Suspend<br>0 = Not Supported, 1 = To Read Only, 2 = To Read & Write |
| 47h | 0001h | Sector Protect<br>0 = Not Supported, X = Number of sectors in per group |
| 48h | 0000h | Sector Temporary Unprotect<br>00 = Not Supported, 01 = Supported |
| 49h | 0008h | Sector Protect/Unprotect scheme<br>0008h = Advanced Sector Protection |
| 4Ah | 0000h | Simultaneous Operation<br>00 = Not Supported, X = Number of Sectors in Bank |
| 4Bh | 0000h | Burst Mode Type<br>00 = Not Supported, 01 = Supported |
| 4Ch | 0002h | Page Mode Type<br>00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page |
| 4Dh | 00B5h | ACC (Acceleration) Supply Minimum<br>00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV |
| 4Eh | 00C5h | ACC (Acceleration) Supply Maximum<br>00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV |
| 4Fh | 0004h/<br>0005h | Top/Bottom Boot Sector Flag<br>00h = Uniform Device without WP# protect, 02h = Bottom Boot Device, 03h = Top Boot Device, 04h = Uniform sectors bottom WP# protect, 05h = Uniform sectors top WP# protect |
| 50h | 0001h | Program Suspend<br>00h = Not Supported, 01h = Supported |

# Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table 10 and Table 11 define the valid register command sequences. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state.* A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the AC Characteristics section for timing diagrams.

## Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

The system *must* issue the reset command to return the device to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the device is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Reading Array Data in the Device Bus Operations section for more information. The Read-Only Operations–"AC Characteristics" section on page 80 provides the read parameters, and Figure 11 shows the timing diagram.

## Reset Command

Writing the reset command resets the device to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to the read mode. If the program command sequence is written while the device is in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If the device entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to the read mode (or erase-suspend-read mode if the device was in Erase Suspend).

Note that if DQ1 goes high during a Write Buffer Programming operation, the system must write the Write-to-Buffer-Abort Reset command sequence to reset the device for the next operation.

## Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Table 10 and Table 11 show the address and data requirements. This method requires $V_{ID}$ on address pin A9. The autoselect command sequence may be written

to an address that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the autoselect command. The device then enters the autoselect mode. The system may read at any address any number of times without initiating another autoselect command sequence:

- A read cycle at address XX00h returns the manufacturer code.
- Three read cycles at addresses 01h, 0Eh, and 0Fh return the device code.
- A read cycle to an address containing a sector address (SA), and the address 02h on A7–A0 in word mode returns 01h if the sector is protected, or 00h if it is unprotected.

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the device was previously in Erase Suspend).

## Enter Secured Silicon Sector/Exit Secured Silicon Sector Command Sequence

The Secured Silicon Sector region provides a secured data area containing an 8-word/16-byte random Electronic Serial Number (ESN). The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence. The Exit Secured Silicon Sector command sequence returns the device to normal operation. Table 10 and Table 11 show the address and data requirements for both command sequences. See also "Secured Silicon Sector Flash Memory Region" for further information. *Note that the ACC function and unlock bypass modes are not available when the Secured Silicon Sector is enabled.*

## Word Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 10 and Table 11 show the address and data requirements for the word program command sequence.

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. Refer to the Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. ***Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when a program operation is in progress.*** Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once the device has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. Programming to the same word address multiple times without intervening erases is limited. For such application requirements, please contact your local Spansion representative. **Any word cannot be programmed from "0" back to a "1."** Attempting to do so may cause the device to set DQ5 = 1, or cause the DQ7 and

DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

### Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 10 and Table 11 show the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. (See Table 10 and Table 11).

### Write Buffer Programming

Write Buffer Programming allows the system write to a maximum of 16 words/32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the Sector Address in which programming will occur. The fourth cycle writes the sector address and the number of word locations, minus one, to be programmed. For example, if the system will program 6 unique address locations, then 05h should be written to the device. This tells the device how many write buffer addresses will be loaded with data and therefore when to expect the Program Buffer to Flash command. The number of locations to program cannot exceed the size of the write buffer or the operation will abort.

The fifth cycle writes the first address location and data to be programmed. The write-buffer-page is selected by address bits $A_{MAX}$–$A_4$. All subsequent address/data pairs must fall within the selected-write-buffer-page. The system then writes the remaining address/data pairs into the write buffer. Write buffer locations may be loaded in any order.

The write-buffer-page address must be the same for all address/data pairs loaded into the write buffer. (This means Write Buffer Programming cannot be performed across multiple write-buffer pages. This also means that Write Buffer Programming cannot be performed across multiple sectors. If the system attempts to load programming data outside of the selected write-buffer page, the operation will abort.)

Note that if a Write Buffer address location is loaded multiple times, the address/data pair counter will be decremented for every data load operation. The host system must therefore account for loading a write-buffer location more than once. The counter decrements for each data load operation, not for each unique write-buffer-address location. Note also that if an address location is loaded more

than once into the buffer, the final data loaded for that address will be programmed.

Once the specified number of write buffer locations have been loaded, the system must then write the Program Buffer to Flash command at the sector address. Any other address and data combination aborts the Write Buffer Programming operation. The device then begins programming. Data polling should be used while monitoring the last address location loaded into the write buffer. DQ7, DQ6, DQ5, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer programming operation can be suspended using the standard program suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device is ready to execute the next command.

The Write Buffer Programming Sequence can be aborted in the following ways:

- Load a value that is greater than the page buffer size during the Number of Locations to Program step.
- Write to an address in a sector different than the one specified during the Write-Buffer-Load command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the Starting Address during the write buffer data loading stage of the operation.
- Write data other than the Confirm Command after the specified number of data load cycles.

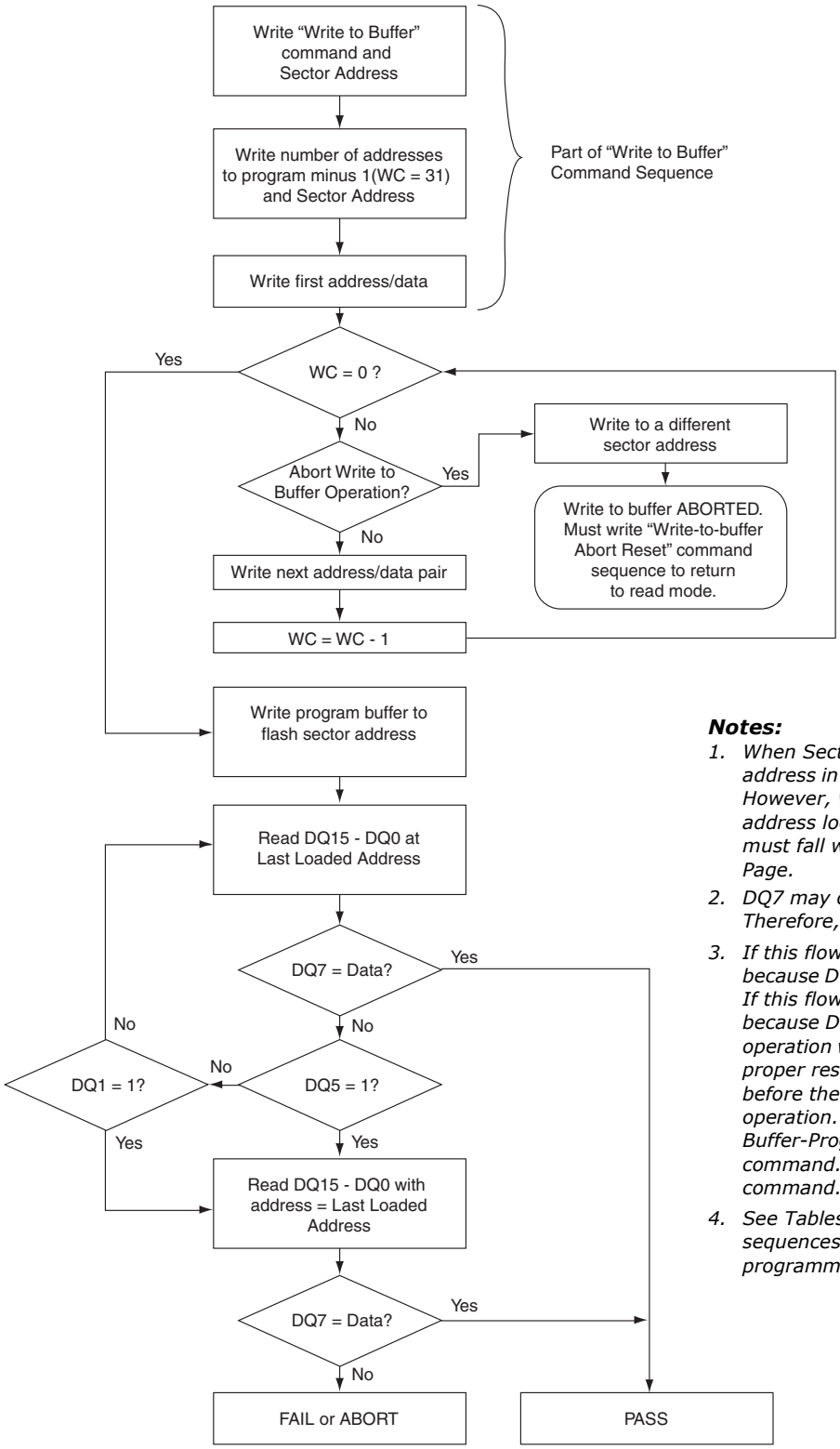
The abort condition is indicated by DQ1 = 1, DQ7 = DATA# (for the last address location loaded), DQ6 = toggle, and DQ5=0. A Write-to-Buffer-Abort Reset command sequence must be written to reset the device for the next operation. Note that the full 3-cycle Write-to-Buffer-Abort Reset command sequence is required when using Write-Buffer-Programming features in Unlock Bypass mode.

Write buffer programming is allowed in any sequence. Note that the Secured Silicon sector, autoselect, and CFI functions are unavailable when a program operation is in progress. This flash device is capable of handling multiple write buffer programming operations on the same write buffer address range without intervening erases. For applications requiring an excessive number of such repeated write buffer programming operations, please contact your local Spansion representative. **Any bit in a write buffer address range cannot be programmed from "0" back to a "1."** Attempting to do so may cause the device to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

### Accelerated Program

The device offers accelerated program operations through the WP#/ACC pin. When the system asserts $V_{HH}$ on the WP#/ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the WP#/ACC pin to accelerate the operation. *Note that the* WP#*/ACC pin must not be at $V_{HH}$ for operations other than accelerated programming, or device damage may result. WP# has an internal pullup; when unconnected, WP# is at $V_{IH}$.*

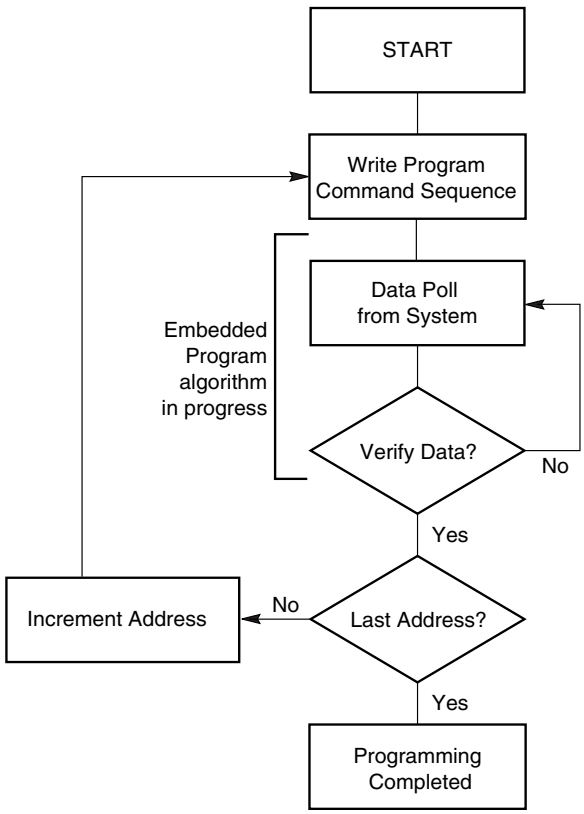
Figure 3 illustrates the algorithm for the program operation. Refer to the Erase and Program Operations–"AC Characteristics" section on page 80 section for parameters, and Figure 14 for timing diagrams.




***Notes:***

1. *When Sector Address is specified, any address in the selected sector is acceptable. However, when loading Write-Buffer address locations with data, all addresses must fall within the selected Write-Buffer Page.*
2. *DQ7 may change simultaneously with DQ5. Therefore, DQ7 should be verified.*
3. *If this flowchart location was reached because DQ5= "1", then the device FAILED. If this flowchart location was reached because DQ1= "1", then the Write to Buffer operation was ABORTED. In either case, the proper reset command must be written before the device can begin another operation. If DQ1=1, write the Write-Buffer-Programming-Abort-Reset command. if DQ5=1, write the Reset command.*
4. *See Tables 16 and 17 for command sequences required for write buffer programming.*

**Figure I. Write Buffer Programming Operation**




***Note:*** *See Table 10 and Table 11 for program command sequence.*

**Figure 2. Program Operation**

## Program Suspend/Program Resume Command Sequence

The Program Suspend command allows the system to interrupt a programming operation or a Write to Buffer programming operation so that data can be read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the program operation within 15 µs maximum (5µs typical) and updates the status bits. Addresses are not required when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the Secured Silicon Sector area (One-time Program area), then user must use the proper command sequences to enter and exit this region.

The system may also write the autoselect command sequence when the device is in the Program Suspend mode. The system can read as many autoselect codes as required. When the device exits the autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See Autoselect Command Sequence for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See Write Operation Status for more information.

The system must write the Program Resume command (address bits are don't care) to exit the Program Suspend mode and continue the programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device has resume programming.

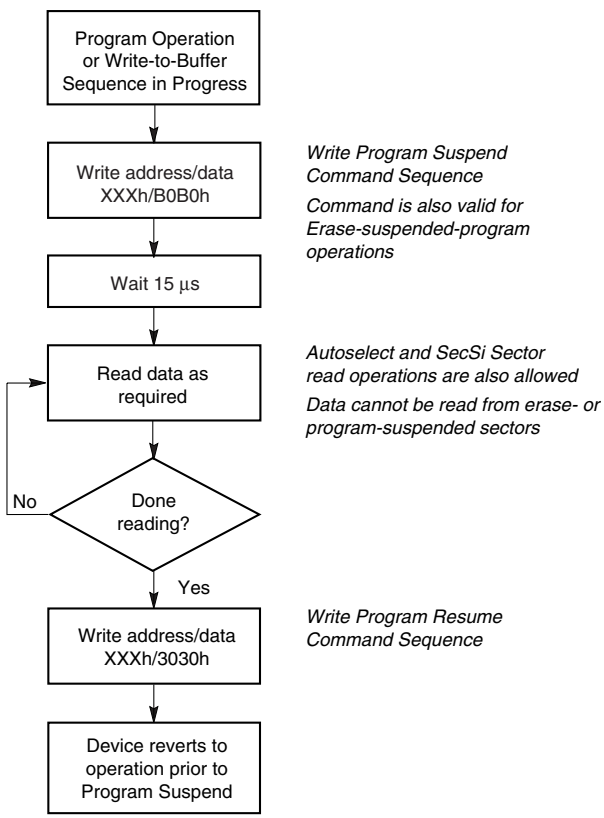



**Figure 3. Program Suspend/Program Resume**

## Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 10 and Table 11 show the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, the device returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. Refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored, including erase suspend commands. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 4 illustrates the algorithm for the erase operation. ***Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when an erase operation in is progress.*** Refer to the Erase and Program Operations table in the AC Characteristics section for parameters, and Figure 16 section for timing diagrams.

## Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 10 and Table 11 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

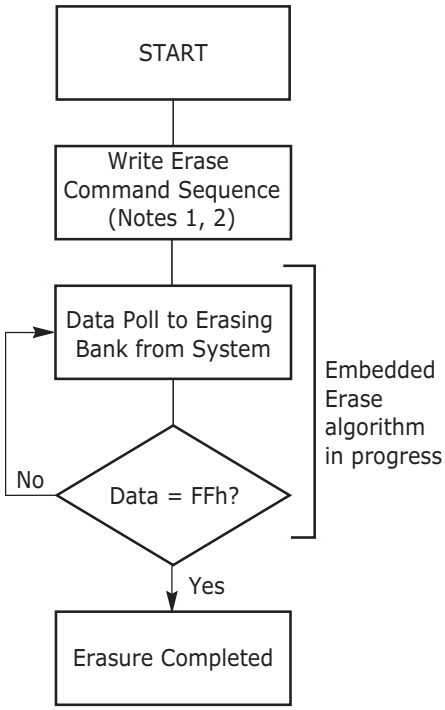
After the command sequence is written, a sector erase time-out of 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to the read mode.** ***Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when an erase operation in is progress.*** The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by reading DQ7, DQ6, or DQ2 in the erasing sector. Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 4 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations table in the AC Characteristics section for parameters, and Figure 16 section for timing diagrams.




***Notes:***
1. *See Table 10 and Table 11 for program command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

**Figure 4. Erase Operation**

## Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a typical of 5 µs (maximum of 20 µs) to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read mode. The system can determine the status of the pro-

gram operation using the DQ7 or DQ6 status bits, just as in the standard word program operation. Refer to the Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the "Autoselect Command Sequence" section on page 50 sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. The address of the erase-suspended sector is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

## Lock Register Command Set Definitions

The Lock Register Command Set permits the user to one-time program the Secured Silicon Sector Protection Bit, Persistent Protection Mode Lock Bit, and Password Protection Mode Lock Bit. The Lock Register bits are all readable after an initial access delay.

The **Lock Register Command Set Entry** command sequence must be issued prior to any of the following commands listed, to enable proper command execution.

Note that issuing the **Lock Register Command Set Entry** command **disables reads and writes for the flash memory**.

- Lock Register Program Command
- Lock Register Read Command

The **Lock Register Command Set Exit** command must be issued after the execution of the commands to reset the device to read mode. Otherwise the device will hang. If this happens, the flash device must be reset. Please refer to RESET# for more information. It is important to note that the device will be in either Persistent Protection mode or Password Protection mode depending on the mode selected prior to the device hang.

For either the Secured Silicon Sector to be locked, or the device to be permanently set to the Persistent Protection Mode or the Password Protection Mode, the associated Lock Register bits must be programmed. **Note that the Persistent Protection Mode Lock Bit and Password Protection Mode Lock Bit can never be programmed together at the same time. If so, the Lock Register Program operation will abort**.

**The Lock Register Command Set Exit command must be initiated to re-enable reads and writes to the main memory.**

## Password Protection Command Set Definitions

The Password Protection Command Set permits the user to program the 64-bit password, verify the programming of the 64-bit password, and then later unlock the device by issuing the valid 64-bit password.

The **Password Protection Command Set Entry** command sequence must be issued prior to any of the following commands listed, to enable proper command execution.

Note that issuing the **Password Protection Command Set Entry** command **disables reads and writes for the main memory**.

- Password Program Command

The Password Program command permits programming the password that is used as part of the hardware protection scheme. The actual password is 64-bits long. There is no special addressing order required for programming the password. **The password is programmed in 8-bit or 16-bit portions. Each portion requires a Password Program Command.**

Once the Password is written and verified, the Password Protection Mode Lock Bit in the "Lock Register" must be programmed in order to prevent verification. The Password Program command is only capable of programming "0"s. Programming a "1" after a cell is programmed as a "0" results in a time-out by the Embedded Program Algorithm™ with the cell remaining as a "0". The password is all F's when shipped from the factory. All 64-bit password combinations are valid as a password.

- Password Read Command

The Password Read command is used to verify the Password. The Password is verifiable only when the Password Protection Mode Lock Bit in the "Lock Register" is not programmed. If the Password Protection Mode Lock Bit in the "Lock Register" is programmed and the user attempts to read the Password, the device will always drive all F's onto the DQ data bus.

The lower two address bits (A1-A0) for word mode and (A1-A-1) for by byte mode are valid during the Password Read, Password Program, and Password Unlock commands. **Writing a "1" to any other address bits ($A_{MAX}$-A2) will abort the Password Read, Password Program, and Password Unlock commands and return the device to reading memory array. The address bits (A1-A0) for word mode and (A1-A-1) for byte mode must be entered into the device sequentially for Password Read and Password Unlock commands**.

- Password Unlock Command

The Password Unlock command is used to clear the PPB Lock Bit to the "unfreeze state" so that the PPB bits can be modified. The exact password must be entered in order for the unlocking function to occur. **This 64-bit Password Unlock command sequence will take at least 2 µs to process each time to prevent a hacker from running through the all 64-bit combinations in an attempt to correctly match a password. If another password unlock is issued before the 64-bit password check execution window is completed, the command will be ignored.**

The Password Unlock function is accomplished by writing Password Unlock command and data to the device to perform the clearing of the PPB Lock Bit to the "unfreeze state". The password is 64 bits long. A1 and A0 are used for matching in word mode and A1, A0, A-1 in byte mode. Writing the Password Unlock command does not need to be address order specific. An example sequence is starting with the lower address A1-A0= 00, followed by A1-A0= 01, A1-A0= 10, and A1-A0= 11 if device is configured to operate in word mode.

**Approximately 2 µs is required for unlocking the device after the valid 64-bit password is given to the device. It is the responsibility of the microprocessor to keep track of the entering the portions of the 64-bit password with the Password Unlock command, the order, and when to read the PPB Lock bit to confirm successful password unlock**. In order to re-lock the device into the Password Protection Mode, the PPB Lock Bit Set command can be re-issued.

**The Password Protection Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode. Otherwise the device will hang.

Note that issuing the **Password Protection Command Set Exit command re-enables reads and writes for the main memory**.

## Non-Volatile Sector Protection Command Set Definitions

The Non-Volatile Sector Protection Command Set permits the user to program the Persistent Protection Bits (PPB bits), erase all of the Persistent Protection Bits (PPB bits), and read the logic state of the Persistent Protection Bits (PPB bits).

The **Non-Volatile Sector Protection Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Note that issuing the **Non-Volatile Sector Protection Command Set Entry** command **disables reads and writes for the main memory**.

- PPB Program Command

The PPB Program command is used to program, or set, a given PPB bit. Each PPB bit is individually programmed (but is bulk erased with the other PPB bits). The specific sector address (A24-A16 for S29GL512N, A23-A16 for S29GL256N, A22-A16 for S29GL128N) is written at the same time as the program command. If the PPB Lock Bit is set to the "freeze state", the PPB Program command will not execute and the command will time-out without programming the PPB bit.

- All PPB Erase Command

The All PPB Erase command is used to erase all PPB bits in bulk. There is no means for individually erasing a specific PPB bit. Unlike the PPB program, no specific sector address is required. However, when the All PPB Erase command is issued, all Sector PPB bits are erased in parallel. If the PPB Lock Bit is set to "freeze state", the ALL PPB Erase command will not execute and the command will time-out without erasing the PPB bits.

The device will preprogram all PPB bits prior to erasing when issuing the All PPB Erase command. Also note that the total number of PPB program/erase cycles has the same endurance as the flash memory array.

- PPB Status Read Command

The programming state of the PPB for a given sector can be verified by writing a PPB Status Read Command to the device. This requires an initial access time latency.

The **Non-Volatile Sector Protection Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode.

Note that issuing the **Non-Volatile Sector Protection Command Set Exit** command **re-enables reads and writes for the main memory**.

## Global Volatile Sector Protection Freeze Command Set

The Global Volatile Sector Protection Freeze Command Set permits the user to set the PPB Lock Bit and reading the logic state of the PPB Lock Bit.

The **Global Volatile Sector Protection Freeze Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution.

**Reads and writes from the main memory are allowed.**

- PPB Lock Bit Set Command

The PPB Lock Bit Set command is used to set the PPB Lock Bit to the "freeze state" if it is cleared either at reset or if the Password Unlock command was successfully executed. There is no PPB Lock Bit Clear command. Once the PPB Lock Bit is set to the "freeze state", it cannot be cleared unless the device is taken through a power-on clear (for Persistent Protection Mode) or the Password Unlock command is executed (for Password Protection Mode). If the Password Protection Mode Lock Bit is programmed, the PPB Lock Bit status is reflected as set to the "freeze state", even after a power-on reset cycle.

- PPB Lock Bit Status Read Command

The programming state of the PPB Lock Bit can be verified by executing a PPB Lock Bit Status Read command to the device.

The **Global Volatile Sector Protection Freeze Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode.

## Volatile Sector Protection Command Set

The Volatile Sector Protection Command Set permits the user to set the Dynamic Protection Bit (DYB) to the "protected state", clear the Dynamic Protection Bit (DYB) to the "unprotected state", and read the logic state of the Dynamic Protection Bit (DYB).

The **Volatile Sector Protection Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution.

Note that issuing the **Volatile Sector Protection Command Set Entry** command **disables reads for the bank selected with the command**. **Reads and Writes for other banks excluding that bank are allowed**.

- DYB Set Command
- DYB Clear Command

The DYB Set and DYB Clear commands are used to protect or unprotect a DYB for a given sector. The high order address bits are issued at the same time as the code 00h or 01h on DQ7-DQ0. All other DQ data bus pins are ignored during the data write cycle. The DYB bits are modifiable at any time, regardless of the state of the PPB bit or PPB Lock Bit. The DYB bits are cleared to the "unprotected state" at power-up or hardware reset.

—DYB Status Read Command

The programming state of the DYB bit for a given sector can be verified by writing a DYB Status Read command to the device. This requires an initial access delay.

The **Volatile Sector Protection Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode.

Note that issuing the **Volatile Sector Protection Command Set Exit command re-enables reads and writes to the main memory**.

## Secured Silicon Sector Entry Command

The Secured Silicon Sector Entry command allows the following commands to be executed

- Read from Secured Silicon Sector
- Program to Secured Silicon Sector

Once the Secured Silicon Sector Entry Command is issued, the Secured Silicon Sector Exit command has to be issued to exit Secured Silicon Sector Mode.

## Secured Silicon Sector Exit Command

The Secured Silicon Sector Exit command may be issued to exit the Secured Silicon Sector Mode.

## Command Definitions

**Table 10. S29GL512N, S29GL256N, S29GL128N Command Definitions, x16**

| Command (Notes) | | Cycles | Bus Cycles (Notes 2–5) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | First | | Second | | Third | | Fourth | | Fifth | | Sixth | |
| | | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Read (6) | | 1 | RA | RD | | | | | | | | | | |
| Reset (7) | | 1 | XXX | F0 | | | | | | | | | | |
| Autoselect (Note 8) | Manufacturer ID | 4 | 555 | AA | 2AA | 55 | 555 | 90 | X00 | 01 | | | | |
| | Device ID | 4 | 555 | AA | 2AA | 55 | 555 | 90 | X01 | 227E | X0E | Note 17 | X0F | Note 17 |
| | Sector Protect Verify | 4 | 555 | AA | 2AA | 55 | 555 | 90 | (SA) X02 | XX00 | | | | |
| | | | | | | | | | | XX01 | | | | |
| | Secure Device Verify (9) | 4 | 555 | AA | 2AA | 55 | 555 | 90 | X03 | Note 10 | | | | |
| CFI Query (11) | | 1 | 555 | 98 | | | | | | | | | | |
| Program | | 4 | 555 | AA | 2AA | 55 | 555 | A0 | PA | PD | | | | |
| Write to Buffer | | 3 | 555 | AA | 2AA | 55 | SA | 25 | SA | WC | PA | PD | WBL | PD |
| Program Buffer to Flash (confirm) | | 1 | SA | 29 | | | | | | | | | | |
| Write-to-Buffer-Abort Reset (16) | | 3 | 555 | AA | 2AA | 55 | 555 | F0 | | | | | | |
| Unlock Bypass | | 3 | 555 | AA | 2AA | 55 | 555 | 20 | | | | | | |
| Unlock Bypass Program (12) | | 2 | XXX | A0 | PA | PD | | | | | | | | |
| Unlock Bypass Sector Erase (12) | | 2 | XXX | 80 | SA | 30 | | | | | | | | |
| Unlock Bypass Chip Erase (12) | | 2 | XXX | 80 | XXX | 10 | | | | | | | | |
| Unlock Bypass Reset (13) | | 2 | XXX | 90 | XXX | 00 | | | | | | | | |
| Chip Erase | | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | 555 | 10 |
| Sector Erase | | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | SA | 30 |
| Erase Suspend/Program Suspend (14) | | 1 | XXX | B0 | | | | | | | | | | |
| Erase Resume/Program Resume (15) | | 1 | XXX | 30 | | | | | | | | | | |
| **Sector Command Definitions** | | | | | | | | | | | | | | |
| Secured Silicon Sector | Secured Silicon Sector Entry | 3 | 555 | AA | 2AA | 55 | 555 | 88 | | | | | | |
| | Secured Silicon Sector Exit (18) | 4 | 555 | AA | 2AA | 55 | 555 | 90 | XX | 00 | | | | |
| **Lock Register Command Set Definitions** | | | | | | | | | | | | | | |
| Lock Register | Lock Register Command Set Entry | 3 | 555 | AA | 2AA | 55 | 555 | 40 | | | | | | |
| | Lock Register Bits Program (22) | 2 | XXX | A0 | XXX | Data | | | | | | | | |
| | Lock Register Bits Read (22) | 1 | 00 | Data | | | | | | | | | | |
| | Lock Register Command Set Exit (18, 23) | 2 | XXX | 90 | XXX | 00 | | | | | | | | |
| **Password Protection Command Set Definitions** | | | | | | | | | | | | | | |

| Command (Notes) | | Cycles | Bus Cycles (Notes 2–5) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | First | | Second | | Third | | Fourth | | Fifth | | Sixth | |
| | | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Password | Password Protection Command Set Entry | 3 | 555 | AA | 2AA | 55 | 555 | 60 | | | | | | |
| | Password Program (20) | 2 | XXX | A0 | PWA x | PWD x | | | | | | | | |
| | Password Read (19) | 4 | XXX | PWD 0 | 01 | PWD 1 | 02 | PWD 2 | 03 | PWD 3 | | | | |
| | Password Unlock (19) | 7 | 00 | 25 | 00 | 03 | 00 | PWD 0 | 01 | PWD 1 | 02 | PWD 2 | 03 | PWD 3 |
| | | | 00 | 29 | | | | | | | | | | |
| | Password Protection Command Set Exit (18, 23) | 2 | XXX | 90 | XXX | 00 | | | | | | | | |
| **Non-Volatile Sector Protection Command Set Definitions** | | | | | | | | | | | | | | |
| PPB | Nonvolatile Sector Protection Command Set Entry | 3 | 555 | AA | 2AA | 55 | 555 | C0 | | | | | | |
| | PPB Program (24, 25) | 2 | XXX | A0 | SA | 00 | | | | | | | | |
| | All PPB Erase | 2 | XXX | 80 | 00 | 30 | | | | | | | | |
| | PPB Status Read (25) | 1 | SA | RD (0) | | | | | | | | | | |
| | Non-Volatile Sector Protection Command Set Exit (18) | 2 | XXX | 90 | XXX | 00 | | | | | | | | |
| **Global Non-Volatile Sector Protection Freeze Command Set Definitions** | | | | | | | | | | | | | | |
| PPB Lock Bit | Global Non-Volatile Sector Protection Freeze Command Set Entry | 3 | 555 | AA | 2AA | 55 | 555 | 50 | | | | | | |
| | PPB Lock Bit Set (25) | 2 | XXX | A0 | XXX | 00 | | | | | | | | |
| | PPB Lock Status Read (25) | 1 | XXX | RD (0) | | | | | | | | | | |
| | Global Non-Volatile Sector Protection Freeze Command Set Exit (18) | 2 | XXX | 90 | XXX | 00 | | | | | | | | |
| **Volatile Sector Protection Command Set Definitions** | | | | | | | | | | | | | | |
| DYB | Volatile Sector Protection Command Set Entry | 3 | 555 | AA | 2AA | 55 | 555 | E0 | | | | | | |
| | DYB Set (24, 25) | 2 | XXX | A0 | SA | 00 | | | | | | | | |
| | DYB Clear (25) | 2 | XXX | A0 | SA | 01 | | | | | | | | |
| | DYB Status Read (25) | 1 | SA | RD (0) | | | | | | | | | | |
| | Volatile Sector Protection Command Set Exit (18) | 2 | XXX | 90 | XXX | 00 | | | | | | | | |

***Legend:***

*X = Don't care*

*RA = Address of the memory to be read.*

*RD = Data read from location RA during read operation.*

*PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.*

*PD = Data to be programmed at location PA. Data latches on the rising edge of the WE# or CE# pulse, whichever happens first.*

*SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits $A_{max}$–A16 uniquely select any sector.*

*WBL = Write Buffer Location. The address must be within the same write buffer page as PA.*

*WC = Word Count is the number of write buffer locations to load minus 1.*

*PWD = Password*

*$PWD_x$ = Password word0, word1, word2, and word3.*

*DATA = Lock Register Contents: PD(0) = Secured Silicon Sector Protection Bit, PD(1) = Persistent Protection Mode Lock Bit, PD(2) = Password Protection Mode Lock Bit.*

***Notes:***

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle, and the 4th, 5th, and 6th cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15-DQ8 are don't cares for unlock and command cycles.*
5. *Address bits $A_{MAX}$:A16 are don't cares for unlock and command cycles, unless SA or PA required. ($A_{MAX}$ is the Highest Address pin.).*
6. *No unlock or command cycles required when reading array data.*
7. *The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).*
8. *The fourth, fifth, and sixth cycle of the autoselect command sequence is a read cycle.*
9. *The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence" for more information. This is same as PPB Status Read except that the protect and unprotect statuses are inverted here.*
10. *The data value for DQ7 is "1" for a serialized and protected OTP region and "0" for an unserialized and unprotected Secured Silicon Sector region. See "Secured Silicon Sector Flash Memory Region" for more information. For Am29LVxxxMH: XX18h/18h = Not Factory Locked. XX98h/98h = Factory Locked. For Am29LVxxxML: XX08h/08h = Not Factory Locked. XX88h/88h = Factory Locked.*
11. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
12. *The Unlock-Bypass command is required prior to the Unlock-Bypass-Program command.*
13. *The Unlock-Bypass-Reset command is required to return to reading array data when the device is in the unlock bypass mode.*
14. *The system may read and program/program suspend in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
15. *The Erase Resume/Program Resume command is valid only during the Erase Suspend/Program Suspend modes.*
16. *Issue this command sequence to return to READ mode after detecting device is in a Write-to-Buffer-Abort state. NOTE: the full command sequence is required if resetting out of ABORT while using Unlock Bypass Mode.*
17. *S29GL512NH/L = 2223h/23h, 220h/01h; S29GL256NH/L = 2222h/22h, 2201h/01h; S29GL128NH/L = 2221h/21h, 2201h/01h.*
18. *The Exit command returns the device to reading the array.*
19. *Note that the password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.*
20. *For PWDx, only one portion of the password can be programmed per each "A0" command.*
21. *The All PPB Erase command embeds programming of all PPB bits before erasure.*
22. *All Lock Register bits are one-time programmable. Note that the program state = "0" and the erase state = "1". Also note that of both the Persistent Protection Mode Lock Bit and the Password Protection Mode Lock Bit cannot be programmed at the same time or the Lock Register Bits Program operation will abort and return the device to read mode. Lock Register bits that are reserved for future use will default to "1's". The Lock Register is shipped out as "FFFF's" before Lock Register Bit program execution.*
23. *If any of the Entry command was initiated, an Exit command must be issued to reset the device into read mode. Otherwise the device will hang.*
24. *If ACC = $V_{HH}$, sector protection will match when ACC = $V_{IH}$*
25. *Protected State = "00h", Unprotected State = "01h".*

## Table II. S29GL5I2N, S29GL256N, S29GLI28N Command Definitions, x8

| Command (Notes) | | Cycles | Bus Cycles (Notes 2–5) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | First | | Second | | Third | | Fourth | | Fifth | | Sixth | |
| | | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Read (6) | | 1 | RA | RD | | | | | | | | | | |
| Reset (7) | | 1 | XXX | F0 | | | | | | | | | | |
| Autoselect | Manufacturer ID | 4 | AAA | AA | 555 | 55 | AAA | 90 | X00 | 01 | | | | |
| | Device ID | 4 | AAA | AA | 555 | 55 | AAA | 9 | X02 | XX7E | X1C | Note 17 | X1E | Note 17 |
| | Sector Protect Verify | 4 | AAA | AA | 555 | 55 | AAA | 90 | (SA) X04 | 00 | | | | |
| | | | | | | | | | | 01 | | | | |
| | Secure Device Verify (9) | 4 | AAA | AA | 555 | 55 | AAA | 90 | X06 | Note 10 | | | | |
| CFI Query (11) | | 1 | AAA | 98 | | | | | | | | | | |
| Write to Buffer | | 3 | AAA | AA | 555 | 55 | SA | 25 | SA | WC | PA | PD | WBL | PD |
| Program Buffer to Flash (confirm) | | 1 | SA | 29 | | | | | | | | | | |
| Write-to-Buffer-Abort Reset (16) | | 3 | AAA | AA | PA | 55 | 555 | F0 | | | | | | |
| Unlock Bypass Reset (13) | | 2 | XXX | 90 | XXX | 00 | | | | | | | | |
| Chip Erase | | 6 | AAA | AA | 555 | 55 | AAA | 80 | AAA | AA | 555 | 55 | AAA | 10 |
| Sector Erase | | 6 | AAA | AA | 555 | 55 | AAA | 80 | AAA | AA | 555 | 55 | SA | 30 |
| Erase Suspend/Program Suspend (14) | | 1 | XXX | B0 | | | | | | | | | | |
| Erase Resume/Program Resume (15) | | 1 | XXX | 30 | | | | | | | | | | |
| **Secured Silicon Sector Command Definitions** | | | | | | | | | | | | | | |
| Secured Silicon Sector | Secured Silicon Sector Entry | 3 | AAA | AA | 555 | 55 | AAA | 88 | | | | | | |
| | Secured Silicon Sector Exit (18) | 4 | AAA | AA | 555 | 55 | AAA | 90 | XX | 00 | | | | |
| **Lock Register Command Set Definitions** | | | | | | | | | | | | | | |
| Lock Register | Lock Register Command Set Entry | 3 | AAA | AA | 555 | 55 | AAA | 40 | | | | | | |
| | Lock Register Bits Program (22) | 2 | XXX | A0 | XXX | Data | | | | | | | | |
| | Lock Register Bits Read (22) | 1 | 00 | Data | | | | | | | | | | |
| | Lock Register Command Set Exit (18, 23) | 2 | XXX | 90 | XXX | 00 | | | | | | | | |
| **Password Protection Command Set Definitions** | | | | | | | | | | | | | | |

| Command (Notes) | | Cycles | Bus Cycles (Notes 2–5) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | First | | Second | | Third | | Fourth | | Fifth | | Sixth | |
| | | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Password | Password Protection Command Set Entry | 3 | AAA | AA | 555 | 55 | AAA | 60 | | | | | | |
| | Password Program (20) | 2 | XXX | A0 | PWA x | PWD x | | | | | | | | |
| | Password Read (19) | 8 | 00 | PWD 0 | 01 | PWD 1 | 02 | PWD 2 | 03 | PWD 3 | 04 | PWD 4 | 05 | PWD 5 |
| | | | 06 | PWD 6 | 07 | PWD 7 | | | | | | | | |
| | Password Unlock (19) | 11 | 00 | 25 | 00 | 03 | 00 | PWD 0 | 01 | PWD 1 | 02 | PWD 2 | 03 | PWD 3 |
| | | | 04 | PWD 4 | 05 | PWD 5 | 06 | PWD 6 | 07 | PWD 7 | 00 | 29 | | |
| | Password Protection Command Set Exit (18, 23) | 2 | XXX | 90 | XXX | 00 | | | | | | | | |
| **Non-Volatile Sector Protection Command Set Definitions** | | | | | | | | | | | | | | |
| PPB | Nonvolatile Sector Protection Command Set Entry | 3 | AAA | AA | 55 | 55 | AAA | C0 | | | | | | |
| | PPB Program (24, 25) | 2 | XXX | A0 | SA | 00 | | | | | | | | |
| | All PPB Erase | 2 | XXX | 80 | 00 | 30 | | | | | | | | |
| | PPB Status Read (25) | 1 | SA | RD (0) | | | | | | | | | | |
| | Non-Volatile Sector Protection Command Set Exit (18) | 2 | XXX | 90 | XXX | 00 | | | | | | | | |
| **Global Non-Volatile Sector Protection Freeze Command Set Definitions** | | | | | | | | | | | | | | |
| PPB Lock Bit | Global Non-Volatile Sector Protection Freeze Command Set Entry | 3 | AAA | AA | 555 | 55 | AAA | 50 | | | | | | |
| | PPB Lock Bit Set (25) | 2 | XXX | A0 | XXX | 00 | | | | | | | | |
| | PPB Lock Status Read (25) | 1 | XXX | RD (0) | | | | | | | | | | |
| | Global Non-Volatile Sector Protection Freeze Command Set Exit (18) | 2 | XXX | 90 | XXX | 00 | | | | | | | | |
| **Volatile Sector Protection Command Set Definitions** | | | | | | | | | | | | | | |
| DYB | Volatile Sector Protection Command Set Entry | 3 | AAA | AA | 555 | 55 | AAA | E0 | | | | | | |
| | DYB Set (24, 25) | 2 | XXX | A0 | SA | 00 | | | | | | | | |
| | DYB Clear (25) | 2 | XXX | A0 | SA | 01 | | | | | | | | |
| | DYB Status Read (25) | 1 | SA | RD (0) | | | | | | | | | | |
| | Volatile Sector Protection Command Set Exit (18) | 2 | XXX | 90 | XXX | 00 | | | | | | | | |

***Legend:***

*X = Don't care*

*RA = Address of the memory to be read.*

*RD = Data read from location RA during read operation.*

*PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.*

*PD = Data to be programmed at location PA. Data latches on the rising edge of the WE# or CE# pulse, whichever happens first.*

*SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits $A_{max}$–A16 uniquely select any sector.*

*WBL = Write Buffer Location. The address must be within the same write buffer page as PA.*

*WC = Word Count is the number of write buffer locations to load minus 1.*

*PWD = Password*

*$PWD_x$ = Password word0, word1, word2, word3. word 4, word 5, word 6, and word 7.*

*DATA = Lock Register Contents: PD(0) = Secured Silicon Sector Protection Bit, PD(1) = Persistent Protection Mode Lock Bit, PD(2) = Password Protection Mode Lock Bit.*

***Notes:***

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle, and the 4th, 5th, and 6th cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15-DQ8 are don't cares for unlock and command cycles.*
5. *Address bits $A_{MAX}$:A16 are don't cares for unlock and command cycles, unless SA or PA required. ($A_{MAX}$ is the Highest Address pin.).*
6. *No unlock or command cycles required when reading array data.*
7. *The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).*
8. *The fourth, fifth, and sixth cycle of the autoselect command sequence is a read cycle.*
9. *The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence" for more information. This is same as PPB Status Read except that the protect and unprotect statuses are inverted here.*
10. *The data value for DQ7 is "1" for a serialized and protected OTP region and "0" for an unserialized and unprotected Secured Silicon Sector region. See "Secured Silicon Sector Flash Memory Region" for more information. For Am29LVxxxMH: XX18h/18h = Not Factory Locked. XX98h/98h = Factory Locked. For Am29LVxxxML: XX08h/08h = Not Factory Locked. XX88h/88h = Factory Locked.*
11. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
12. *The Unlock-Bypass command is required prior to the Unlock-Bypass-Program command.*
13. *The Unlock-Bypass-Reset command is required to return to reading array data when the device is in the unlock bypass mode.*
14. *The system may read and program/program suspend in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
15. *The Erase Resume/Program Resume command is valid only during the Erase Suspend/Program Suspend modes.*
16. *Issue this command sequence to return to READ mode after detecting device is in a Write-to-Buffer-Abort state. NOTE: the full command sequence is required if resetting out of ABORT while using Unlock Bypass Mode.*
17. *S29GL512NH/L = 2223h/23h, 220h/01h; S29GL256NH/L = 2222h/22h, 2201h/01h; S29GL128NH/L = 2221h/21h, 2201h/01h.*
18. *The Exit command returns the device to reading the array.*
19. *Note that the password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.*
20. *For PWDx, only one portion of the password can be programmed per each "A0" command.*
21. *The All PPB Erase command embeds programming of all PPB bits before erasure.*
22. *All Lock Register bits are one-time programmable. Note that the program state = "0" and the erase state = "1". Also note that of both the Persistent Protection Mode Lock Bit and the Password Protection Mode Lock Bit cannot be programmed at the same time or the Lock Register Bits Program operation will abort and return the device to read mode. Lock Register bits that are reserved for future use will default to "1's". The Lock Register is shipped out as "FFFF's" before Lock Register Bit program execution.*
23. *If any of the Entry command was initiated, an Exit command must be issued to reset the device into read mode. Otherwise the device will hang.*
24. *If ACC = $V_{HH}$, sector protection will match when ACC = $V_{IH}$*

*Protected State = "00h", Unprotected State = "01h".*

## Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 19 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress.

The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

Note that all Write Operation Status DQ bits are valid only after 4 µs delay.

## DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

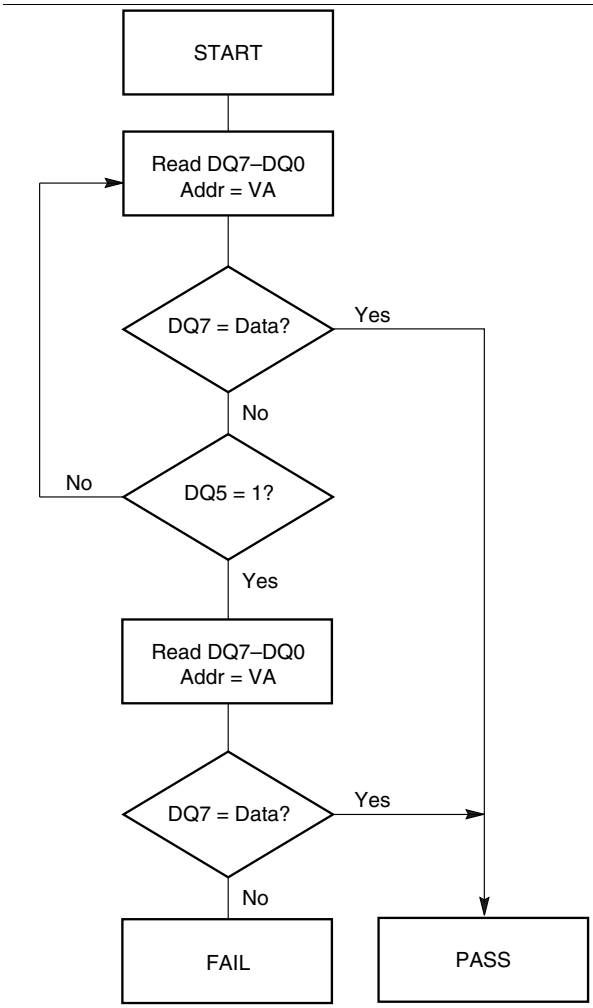
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a "1" on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ0–DQ6 may be still invalid. Valid data on DQ0–DQ7 will appear on successive read cycles.

Table 12 shows the outputs for Data# Polling on DQ7. Figure 5 shows the Data# Polling algorithm. Figure 17 in the AC Characteristics section shows the Data# Polling timing diagram.




***Notes:***

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

**Figure 5. Data# Polling Algorithm**

## RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to $V_{CC}$.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or in the erase-suspend-read mode. Table 12 shows the outputs for RY/BY#.

## DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

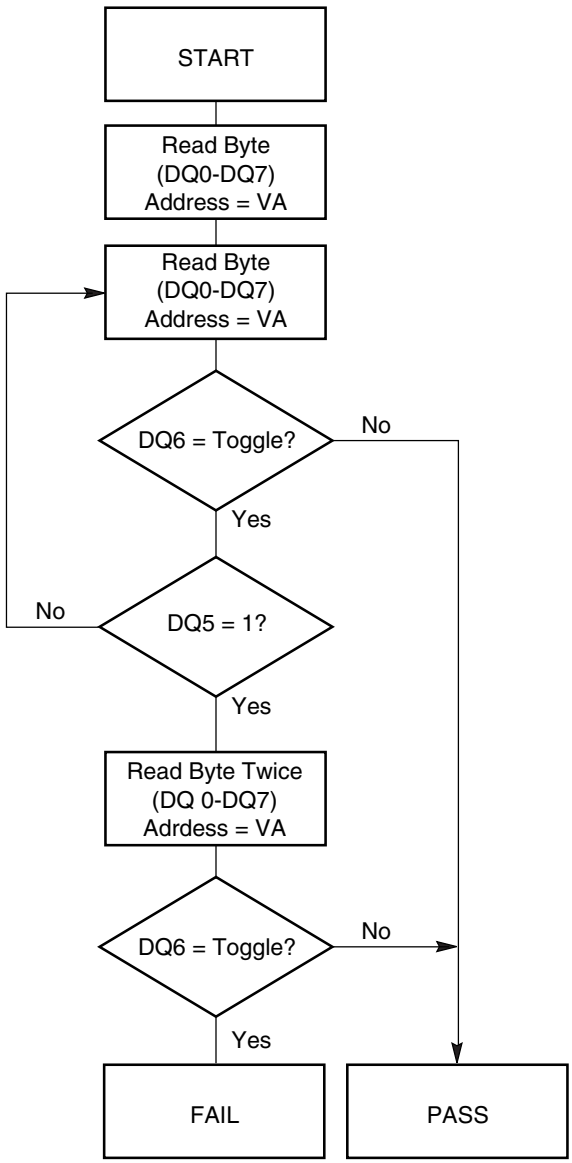
The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 12 shows the outputs for Toggle Bit I on DQ6. Figure 6 shows the toggle bit algorithm. Figure 18 in the "AC Characteristics" section shows the toggle bit tim-

ing diagrams. Figure 19 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.




***Note:*** *The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See the subsections on DQ6 and DQ2 for more information.*

**Figure 6. Toggle Bit Algorithm**

## DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the

read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 12 to compare outputs for DQ2 and DQ6.

Figure 6 shows the toggle bit algorithm in flowchart form, and the section "DQ2: Toggle Bit II" explains the algorithm. See also the RY/BY#: Ready/Busy# subsection. Figure 18 shows the toggle bit timing diagram. Figure 19 shows the differences between DQ2 and DQ6 in graphical form.

## Reading Toggle Bits DQ6/DQ2

Refer to Figure 6 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 6).

## DQ5: Exceeded Timing Limits

DQ5 indicates whether the program, erase, or write-to-buffer time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1."

In all these cases, the system must write the reset command to return the device to the reading the array (or to erase-suspend-read if the device was previously in the erase-suspend-program mode).

## DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a "0" to a "1." If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is "1," the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0," the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 12 shows the status of DQ3 relative to the other status bits.

## DQ1: Write-to-Buffer Abort

DQ1 indicates whether a Write-to-Buffer operation was aborted. Under these conditions DQ1 produces a "1". The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data. See Write Buffer section for more details.

**Table 12. Write Operation Status**

| Status | | | DQ7 (Note 2) | DQ6 | DQ5 (Note 1) | DQ3 | DQ2 (Note 2) | DQ1 | RY/BY# |
|---|---|---|---|---|---|---|---|---|---|
| Standard Mode | Embedded Program Algorithm | | DQ7# | Toggle | 0 | N/A | No toggle | 0 | 0 |
| | Embedded Erase Algorithm | | 0 | Toggle | 0 | 1 | Toggle | N/A | 0 |
| Program Suspend Mode | Program-Suspend Read | Program-Suspended Sector | Invalid (not allowed) | | | | | | 1 |
| | | Non-Program Suspended Sector | Data | | | | | | 1 |
| Erase Suspend Mode | Erase-Suspend Read | Erase-Suspended Sector | 1 | No toggle | 0 | N/A | Toggle | N/A | 1 |
| | | Non-Erase Suspended Sector | Data | | | | | | 1 |
| | Erase-Suspend-Program (Embedded Program) | | DQ7# | Toggle | 0 | N/A | N/A | N/A | 0 |
| Write-to-Buffer | Busy (Note 3) | | DQ7# | Toggle | 0 | N/A | N/A | 0 | 0 |
| | Abort (Note 4) | | DQ7# | Toggle | 0 | N/A | N/A | 1 | 0 |

***Notes:***

1. *DQ5 switches to '1' when an Embedded Program, Embedded Erase, or Write-to-Buffer operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *The Data# Polling algorithm should be used to monitor the last loaded write-buffer address location.*
4. *DQ1 switches to '1' when the device has aborted the write-to-buffer operation*

## Absolute Maximum Ratings

Storage Temperature, Plastic Packages . . . . . −65°C to +150°C

Ambient Temperature with Power Applied . . . . . −65°C to +125°C

Voltage with Respect to Ground:

$V_{CC}$ (Note 1) . . . . . −0.5 V to +4.0 V

$V_{IO}$ . . . . . −0.5 V to +4.0 V

A9, OE#, ACC and RESET# (Note 2) . . . . . −0.5 V to +12.5 V

All other pins (Note 1) . . . . . −0.5 V to $V_{CC}$+12.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

***Notes:***

1. *Minimum DC voltage on input or I/Os is −0.5 V. During voltage transitions, inputs or I/Os may overshoot $V_{SS}$ to −2.0 V for periods of up to 20 ns. See Figure 7. Maximum DC voltage on input or I/Os is $V_{CC}$ + 0.5 V. During voltage transitions, input or I/O pins may overshoot to $V_{CC}$ + 2.0 V for periods up to 20 ns. See Figure 8.*
2. *Minimum DC input voltage on pins A9, OE#, ACC, and RESET# is −0.5 V. During voltage transitions, A9, OE#, ACC, and RESET# may overshoot $V_{SS}$ to −2.0 V for periods of up to 20 ns. See Figure 7. Maximum DC input voltage on pin A9, OE#, ACC, and RESET# is +12.5 V which may overshoot to +14.0V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation*

*of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

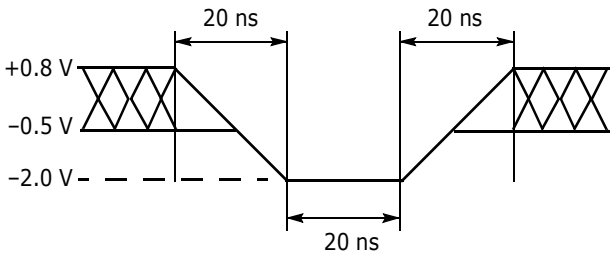



**Figure 7. Maximum Negative Overshoot Waveform**

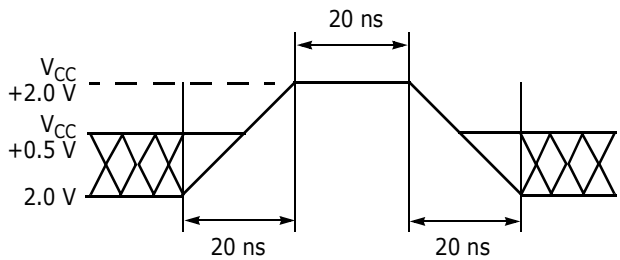



**Figure 8. Maximum Positive Overshoot Waveform**

## Operating Ranges

### Industrial (I) Devices

Ambient Temperature ($T_A$) . . . . . –40°C to +85°C

### Supply Voltages

$V_{CC}$ . . . . . +2.7 V to +3.6 V

$V_{IO}$ (Note 2) . . . . . +1.65 V to +1.95 V or +2.7 to 3.6 V

***Notes:***

1. *Operating ranges define those limits between which the functionality of the device is guaranteed.*
2. *The I/Os will not operate at 3 V when $V_{IO}$=1.8 V.*

# DC Characteristics

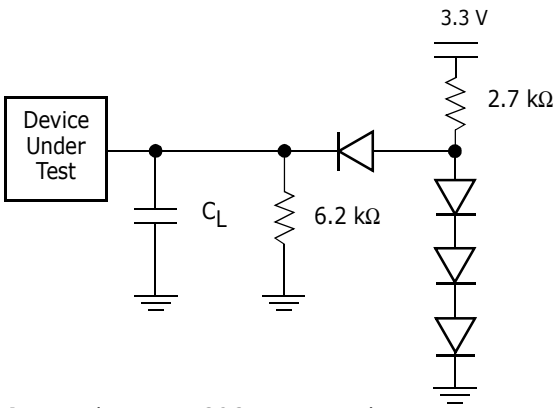
## CMOS Compatible

| Parameter Symbol | Parameter Description (Notes) | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current (1) | $V_{IN} = V_{SS}$ to $V_{CC}$, $V_{CC} = V_{CC\ max}$ | | | ±1.0 | µA |
| $I_{LIT}$ | A9 Input Load Current | $V_{CC} = V_{CC\ max}$; A9 = 12.5 V | | | 35 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT} = V_{SS}$ to $V_{CC}$, $V_{CC} = V_{CC\ max}$ | | | ±1.0 | µA |
| $I_{IO1}$ | $V_{IO}$ Active Read Current (Switching Current) | $V_{IO}$ = 1.8 V, CE# = $V_{IL}$, OE# = $V_{IL}$, WE# = $V_{IL}$, *f* = 5 MHz | | 5 | 10 | µA |
| $I_{IO2}$ | $V_{IO}$ Non-Active Output | CE# = $V_{IL}$, OE# = $V_{IH}$ | | 0.2 | 10 | mA |
| $I_{CC1}$ | $V_{CC}$ Active Read Current (1) | CE# = $V_{IL}$, OE# = $V_{IH}$, $V_{CC} = V_{CCmax}$, *f* = 5 MHz, Byte Mode | | 25 | 30 | mA |
| | | CE# = $V_{IL}$, OE# = $V_{IH}$, $V_{CC} = V_{CCmax}$, *f* = 5 MHz, Word Mode | | 25 | 30 | |
| $I_{CC2}$ | $V_{CC}$ Initial Page Read Current (1) | CE# = $V_{IL}$, OE# = $V_{IH}$, $V_{CC} = V_{CCmax}$ | | 50 | 60 | mA |
| $I_{CC3}$ | $V_{CC}$ *Intra-Page Read Current* (1) | CE# = $V_{IL}$, OE# = $V_{IH}$, $V_{CC} = V_{CCmax}$ | | 10 | 20 | mA |
| $I_{CC4}$ | $V_{CC}$ Active Erase/Program Current (2, 3) | CE# = $V_{IL}$, OE# = $V_{IH}$, $V_{CC} = V_{CCmax}$ | | 50 | 60 | mA |
| $I_{CC5}$ | $V_{CC}$ Standby Current | CE#, RESET# = $V_{SS}$ ± 0.3 V, OE# = $V_{IH}$, $V_{CC} = V_{CCmax}$ | | 1 | 5 | µA |
| $I_{CC6}$ | $V_{CC}$ Reset Current | $V_{CC} = V_{CCmax}$; RESET# = $V_{SS}$ ± 0.3 V | | 1 | 5 | µA |
| $I_{CC7}$ | Automatic Sleep Mode (4) | $V_{CC} = V_{CCmax}$ $V_{IH} = V_{CC}$ ± 0.3 V, $V_{IL} = V_{SS}$ ± 0.3 V, WP#/ACC = $V_{IH}$ | | 1 | 5 | µA |
| $I_{ACC}$ | ACC Accelerated Program Current | CE# = $V_{IL}$, OE# = $V_{IH}$, $V_{CC} = V_{CCmax}$, WP#/ACC = $V_{IH}$ | WP#/ACC pin | 10 | 20 | mA |
| | | | $V_{CC}$ pin | 30 | 60 | |
| $V_{IL}$ | Input Low Voltage (5) | | –0.5 | | 0.3 x $V_{IO}$ | V |
| $V_{IH}$ | Input High Voltage (5) | | 0.7 x $V_{IO}$ | | $V_{IO}$ + 0.3 | V |
| $V_{HH}$ | Voltage for ACC Erase/Program Acceleration | $V_{CC}$ = 2.7 –3.6 V | 11.5 | | 12.5 | V |
| $V_{ID}$ | Voltage for Autoselect and Temporary Sector Unprotect | $V_{CC}$ = 2.7 –3.6 V | 11.5 | | 12.5 | V |
| $V_{OL}$ | Output Low Voltage (5) | $I_{OL}$ = 100 µA | | | 0.15 x $V_{IO}$ | V |
| $V_{OH}$ | Output High Voltage (5) | $I_{OH}$ = 100 µA | 0.85 x $V_{IO}$ | | | V |
| $V_{LKO}$ | Low $V_{CC}$ Lock-Out Voltage (3) | | 2.3 | | 2.5 | V |

***Notes:***

1. *The $I_{CC}$ current listed is typically less than TBD mA/MHz, with OE# at $V_{IH}$.*
2. *$I_{CC}$ active while Embedded Erase or Embedded Program or Write Buffer Programming is in progress.*
3. *Not 100% tested.*
4. *Automatic sleep mode enables the lower power mode when addresses remain stable tor $t_{ACC}$ + 30 ns.*
5. *$V_{IO}$ = 1.65–3.6 V*
6. *$V_{CC}$ = 3 V and $V_{IO}$ = 3V or 1.8V. When $V_{IO}$ is at 1.8V, I/O pins cannot operate at 3V.*

## Test Conditions




***Note:*** *Diodes are IN3064 or equivalent.*

**Figure 9. Test Setup**

**Table 13. Test Specifications**

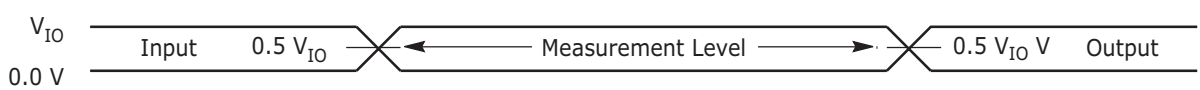
| Test Condition | All Speeds | Unit |
|---|---|---|
| Output Load | 1 TTL gate | |
| Output Load Capacitance, $C_L$ (including jig capacitance) | 30 | pF |
| Input Rise and Fall Times | 5 | ns |
| Input Pulse Levels | 0.0–$V_{IO}$ | V |
| Input timing measurement reference levels (See Note) | 0.5$V_{IO}$ | V |
| Output timing measurement reference levels | 0.5 $V_{IO}$ | V |

***Note:*** *Diodes are IN3064 or equivalent*

***Note:*** *If $V_{IO}$ < $V_{CC}$, the reference level is 0.5 $V_{IO}$.*

## Key to Switching Waveforms

| Waveform | Inputs | Outputs |
|---|---|---|
| | Steady | |
| | Changing from H to L | |
| | Changing from L to H | |
| | Don't Care, Any Change Permitted | Changing, State Unknown |
| | Does Not Apply | Center Line is High Impedance State (High Z) |




***Note:*** *If $V_{IO}$ < $V_{CC}$, the input measurement reference level is 0.5 $V_{IO}$.*

**Figure 10. Input Waveforms and Measurement Levels**

# AC Characteristics

## Read-Only Operations–S29GL5I2N Only

| Parameter | | Description | | Test Setup | | Speed Options | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Std. | | | | | 90 | 100 | 100 | 110 | |
| $t_{AVAV}$ | $t_{RC}$ | Read Cycle Time | | $V_{IO} = V_{CC} = 3$ V | Min | 90 | 100 | | | ns |
| | | | | $V_{IO} = 2.5$ V, $V_{CC} = 3$ V (Note 1) | | 100 | 110 | | | |
| | | | | $V_{IO} = 1.8$ V, $V_{CC} = 3$ V | | | | 100 | 110 | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Address to Output Delay (Note 2) | | $V_{IO} = V_{CC} = 3$ V | Max | 90 | 100 | | | ns |
| | | | | $V_{IO} = 2.5$ V, $V_{CC} = 3$ V (Note 1) | | 100 | 110 | | | |
| | | | | $V_{IO} = 1.8$ V, $V_{CC} = 3$ V | | | | 100 | 110 | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable to Output Delay (Note 3) | | $V_{IO} = V_{CC} = 3$ V | Max | 90 | 105 | | | ns |
| | | | | $V_{IO} = 2.5$ V, $V_{CC} = 3$ V (Note 1) | | 100 | 110 | | | |
| | | | | $V_{IO} = 1.8$ V, $V_{CC} = 3$ V | | | | 100 | 110 | ns |
| | $t_{PACC}$ | Page Access Time | | | Max | 25 | 25 | 35 | 35 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable to Output Delay | | | Max | 25 | 25 | 35 | 35 | ns |
| $t_{EHQZ}$ | $t_{DF}$ | Chip Enable to Output High Z (Note 1) | | | Max | 20 | | | | ns |
| $t_{GHQZ}$ | $t_{DF}$ | Output Enable to Output High Z (Note 1) | | | Max | 20 | | | | ns |
| $t_{AXQX}$ | $t_{OH}$ | Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First | | | Min | 0 | | | | ns |
| | $t_{OEH}$ | Output Enable Hold Time (Note 1) | Read | | Min | 0 | | | | ns |
| | | | Toggle and Data# Polling | | Min | 10 | | | | ns |

***Notes:***

1. *Not 100% tested.*
2. *CE#, OE# = $V_{IL}$*
3. *OE# = $V_{IL}$*
4. *See Figure 9 and Table 13 for test specifications.*
5. *Unless otherwise indicated, AC specifications for 90 ns and 100 ns speed options are tested with $V_{IO} = V_{CC} = 3$ V. AC specifications for 100 ns and 110 ns speed options are tested with $V_{IO} = 1.8$ V and $V_{CC} = 3.0$ V.*

# AC Characteristics

## Read-Only Operations–S29GL256N Only

| Parameter | | Description | | Test Setup | | Speed Options | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Std. | | | | | 80 | 90 | 90 | 100 | |
| $t_{AVAV}$ | $t_{RC}$ | Read Cycle Time | | $V_{IO} = V_{CC} = 3$ V | Min | 80 | 90 | | | ns |
| | | | | $V_{IO} = 2.5$ V, $V_{CC} = 3$ V (Note 1) | | 90 | 100 | | | |
| | | | | $V_{IO} = 1.8$ V, $V_{CC} = 3$ V | | | | 90 | 100 | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Address to Output Delay (Note 2) | | $V_{IO} = V_{CC} = 3$ V | Max | 80 | 90 | | | ns |
| | | | | $V_{IO} = 2.5$ V, $V_{CC} = 3$ V (Note 1) | | 90 | 100 | | | |
| | | | | $V_{IO} = 1.8$ V, $V_{CC} = 3$ V | | | | 90 | 100 | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable to Output Delay (Note 3) | | $V_{IO} = V_{CC} = 3$ V | Max | 80 | 90 | | | ns |
| | | | | $V_{IO} = 2.5$ V, $V_{CC} = 3$ V (Note 1) | | 90 | 100 | | | |
| | | | | $V_{IO} = 1.8$ V, $V_{CC} = 3$ V | | | | 90 | 100 | ns |
| | $t_{PACC}$ | Page Access Time | | | Max | 25 | 25 | 35 | 35 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable to Output Delay | | | Max | 25 | 25 | 35 | 35 | ns |
| $t_{EHQZ}$ | $t_{DF}$ | Chip Enable to Output High Z (Note 1) | | | Max | 20 | | | | ns |
| $t_{GHQZ}$ | $t_{DF}$ | Output Enable to Output High Z (Note 1) | | | Max | 20 | | | | ns |
| $t_{AXQX}$ | $t_{OH}$ | Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First | | | Min | 0 | | | | ns |
| | $t_{OEH}$ | Output Enable Hold Time (Note 1) | Read | | Min | 0 | | | | ns |
| | | | Toggle and Data# Polling | | Min | 10 | | | | ns |

***Notes:***

1. *Not 100% tested.*
2. *CE#, OE# = $V_{IL}$*
3. *OE# = $V_{IL}$*
4. *See Figure 9 and Table 13 for test specifications.*
5. *Unless otherwise indicated, AC specifications for 80 ns and 90 ns speed options are tested with $V_{IO} = V_{CC} = 3$ V. AC specifications for 90 ns and 100 ns speed options are tested with $V_{IO} = 1.8$ V and $V_{CC} = 3.0$ V.*

# AC Characteristics

## Read-Only Operations–S29GLI28N Only

| Parameter | | Description | | Test Setup | | Speed Options | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Std. | | | | | 80 | 90 | 90 | 100 | |
| $t_{AVAV}$ | $t_{RC}$ | Read Cycle Time | | $V_{IO} = V_{CC} = 3$ V | Min | 80 | 90 | | | ns |
| | | | | $V_{IO} = 2.5$ V, $V_{CC} = 3$ V (Note 1) | | 90 | 100 | | | |
| | | | | $V_{IO} = 1.8$ V, $V_{CC} = 3$ V | | | | 90 | 100 | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Address to Output Delay (Note 2) | | $V_{IO} = V_{CC} = 3$ V | Max | 80 | 90 | | | ns |
| | | | | $V_{IO} = 2.5$ V, $V_{CC} = 3$ V (Note 1) | | 90 | 100 | | | |
| | | | | $V_{IO} = 1.8$ V, $V_{CC} = 3$ V | | | | 90 | 100 | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable to Output Delay (Note 3) | | $V_{IO} = V_{CC} = 3$ V | Max | 80 | 90 | | | ns |
| | | | | $V_{IO} = 2.5$ V, $V_{CC} = 3$ V (Note 1) | | 90 | 100 | | | |
| | | | | $V_{IO} = 1.8$ V, $V_{CC} = 3$ V | | | | 90 | 100 | ns |
| | $t_{PACC}$ | Page Access Time | | | Max | 25 | 25 | 35 | 35 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable to Output Delay | | | Max | 25 | 25 | 35 | 35 | ns |
| $t_{EHQZ}$ | $t_{DF}$ | Chip Enable to Output High Z (Note 1) | | | Max | 20 | | | | ns |
| $t_{GHQZ}$ | $t_{DF}$ | Output Enable to Output High Z (Note 1) | | | Max | 20 | | | | ns |
| $t_{AXQX}$ | $t_{OH}$ | Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First | | | Min | 0 | | | | ns |
| | $t_{OEH}$ | Output Enable Hold Time (Note 1) | Read | | Min | 0 | | | | ns |
| | | | Toggle and Data# Polling | | Min | 10 | | | | ns |

***Notes:***

1. *Not 100% tested.*
2. *CE#, OE# = $V_{IL}$*
3. *OE# = $V_{IL}$*
4. *See Figure 9 and Table 13 for test specifications.*
5. *Unless otherwise indicated, AC specifications for 80 ns and 90 ns speed options are tested with $V_{IO} = V_{CC} = 3$ V. AC specifications for 90 ns and 100 ns speed options are tested with $V_{IO} = 1.8$ V and $V_{CC} = 3.0$ V.*

## AC Characteristics

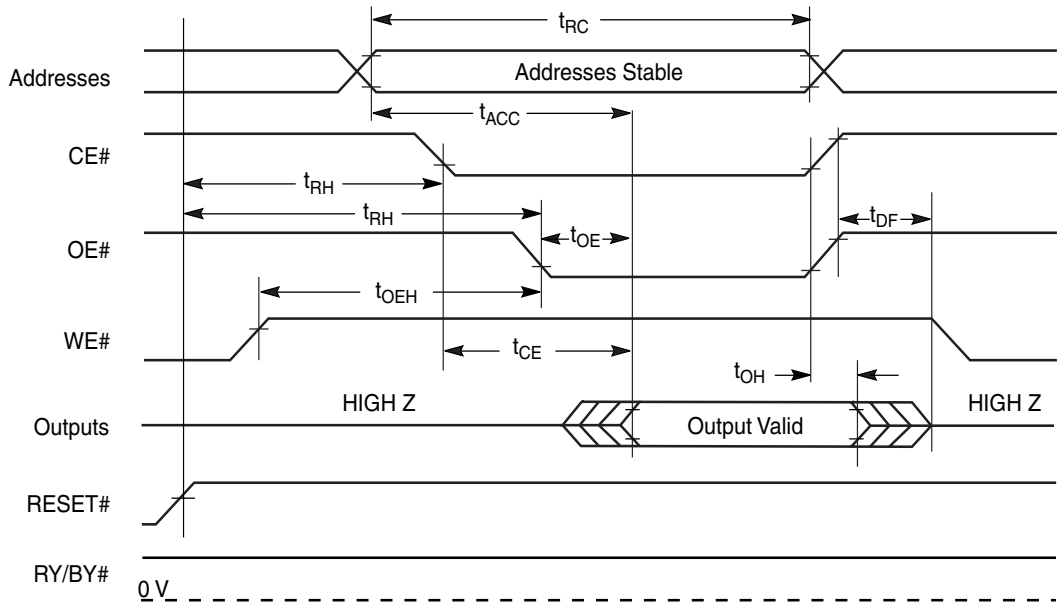
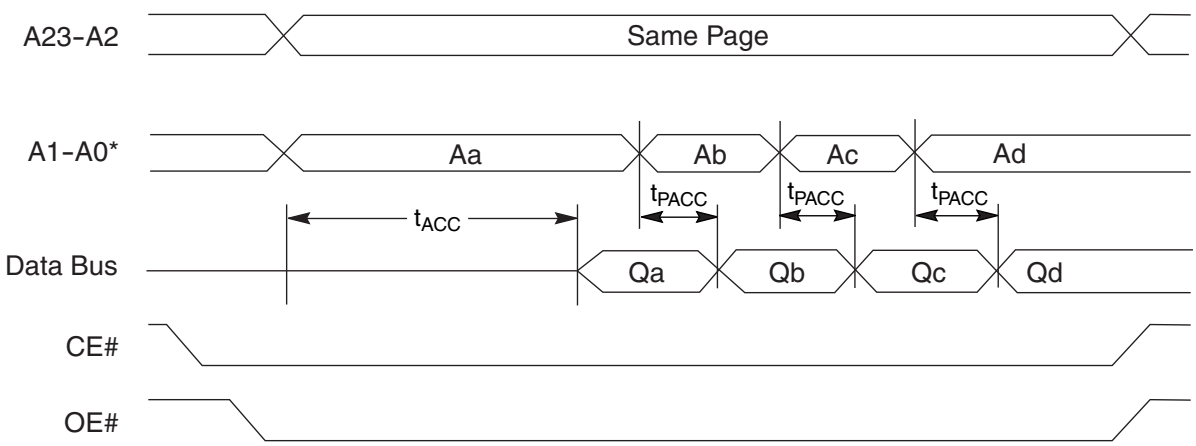



**Figure 11. Read Operation Timings**




***Note:*** *Figure shows word mode. Addresses are A2–A-1 for byte mode.*

**Figure 12. Page Read Timings**

# AC Characteristics

## Hardware Reset (RESET#)

| Parameter | | Description | | All Speed Options | Unit |
|---|---|---|---|---|---|
| JEDEC | Std. | | | | |
| | $t_{Ready}$ | RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note) | Max | 1 | ms |
| | $t_{Ready}$ | RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note) | Max | 1 | ms |
| | $t_{RP}$ | RESET# Pulse Width | Min | 1 | ms |
| | $t_{RH}$ | Reset High Time Before Read (See Note) | Min | 50 | ns |
| | $t_{RPD}$ | RESET# Low to Standby Mode | Min | 20 | µs |
| | $t_{RB}$ | RY/BY# Recovery Time | Min | 0 | ns |

***Note:*** *Not 100% tested. If ramp rate is equal to or faster than 1V/100µs with a falling edge of the RESET# pin initiated, the RESET# pin needs to be held low only for 100µs for power-up.*

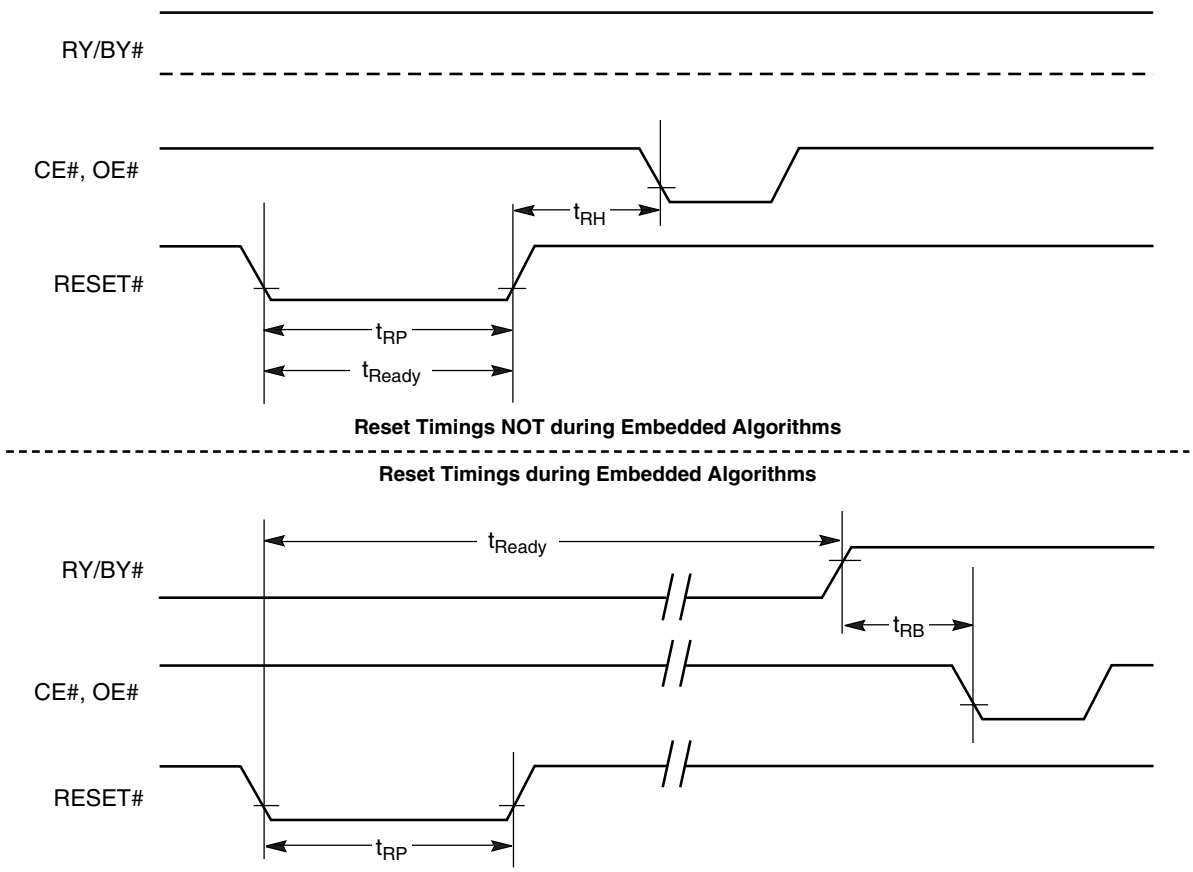



**Figure 13. Reset Timings**

# AC Characteristics

## Erase and Program Operations–S29GL5I2N Only

| Parameter | | Description | | | Speed Options | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Std. | | | | 90 | 100 | 100 | 110 | |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time (Note 1) | | Min | 90 | 100 | 100 | 110 | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Setup Time | | Min | 0 | | | | ns |
| | $t_{ASO}$ | Address Setup Time to OE# low during toggle bit polling | | Min | 15 | | | | ns |
| $t_{WLAX}$ | $t_{AH}$ | Address Hold Time | | Min | 45 | | | | ns |
| | $t_{AHT}$ | Address Hold Time From CE# or OE# high during toggle bit polling | | Min | 0 | | | | ns |
| $t_{DVWH}$ | $t_{DS}$ | Data Setup Time | | Min | 45 | | | | ns |
| $t_{WHDX}$ | $t_{DH}$ | Data Hold Time | | Min | 0 | | | | ns |
| | $t_{OEPH}$ | Output Enable High during toggle bit polling | | Min | 20 | | | | ns |
| $t_{GHWL}$ | $t_{GHWL}$ | Read Recovery Time Before Write (OE# High to WE# Low) | | Min | 0 | | | | ns |
| $t_{ELWL}$ | $t_{CS}$ | CE# Setup Time | | Min | 0 | | | | ns |
| $t_{WHEH}$ | $t_{CH}$ | CE# Hold Time | | Min | 0 | | | | ns |
| $t_{WLWH}$ | $t_{WP}$ | Write Pulse Width | | Min | 35 | | | | ns |
| $t_{WHDL}$ | $t_{WPH}$ | Write Pulse Width High | | Min | 30 | | | | ns |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Write Buffer Program Operation (Notes 2, 3) | | Typ | TBD | | | | µs |
| | | Effective Write Buffer Program Operation (Notes 2, 4) | Per Word | Typ | TBD | | | | µs |
| | | Accelerated Effective Write Buffer Program Operation (Notes 2, 4) | Per Word | Typ | TBD | | | | µs |
| | | Program Operation (Note 2) | Word | Typ | TBD | | | | µs |
| | | Accelerated Programming Operation (Note 2) | Word | Typ | TBD | | | | µs |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Note 2) | | Typ | TBD | | | | sec |
| | $t_{VHH}$ | $V_{HH}$ Rise and Fall Time (Note 1) | | Min | 250 | | | | ns |
| | $t_{VCS}$ | $V_{CC}$ Setup Time (Note 1) | | Min | 50 | | | | µs |

***Notes:***

1. *Not 100% tested.*
2. *See the "AC Characteristics" section for more information.*
3. *For 1–16 words/1–32 bytes programmed.*
4. *Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.*
5. *Unless otherwise indicated, AC specifications for 90 ns and 100 ns speed options are tested with $V_{IO}$ = $V_{CC}$ = 3 V. AC specifications for 100 ns and 110 ns speed options are tested with $V_{IO}$ = 1.8 V and $V_{CC}$ = 3.0 V.*

# AC Characteristics

## Erase and Program Operations–S29GL256N Only

| Parameter | | Description | | | Speed Options | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Std. | | | | 80 | 90 | 90 | 100 | |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time (Note 1) | | Min | 80 | 90 | 90 | 100 | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Setup Time | | Min | 0 | | | | ns |
| | $t_{ASO}$ | Address Setup Time to OE# low during toggle bit polling | | Min | 15 | | | | ns |
| $t_{WLAX}$ | $t_{AH}$ | Address Hold Time | | Min | 45 | | | | ns |
| | $t_{AHT}$ | Address Hold Time From CE# or OE# high during toggle bit polling | | Min | 0 | | | | ns |
| $t_{DVWH}$ | $t_{DS}$ | Data Setup Time | | Min | 45 | | | | ns |
| $t_{WHDX}$ | $t_{DH}$ | Data Hold Time | | Min | 0 | | | | ns |
| | $t_{OEPH}$ | Output Enable High during toggle bit polling | | Min | 20 | | | | ns |
| $t_{GHWL}$ | $t_{GHWL}$ | Read Recovery Time Before Write (OE# High to WE# Low) | | Min | 0 | | | | ns |
| $t_{ELWL}$ | $t_{CS}$ | CE# Setup Time | | Min | 0 | | | | ns |
| $t_{WHEH}$ | $t_{CH}$ | CE# Hold Time | | Min | 0 | | | | ns |
| $t_{WLWH}$ | $t_{WP}$ | Write Pulse Width | | Min | 35 | | | | ns |
| $t_{WHDL}$ | $t_{WPH}$ | Write Pulse Width High | | Min | 30 | | | | ns |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Write Buffer Program Operation (Notes 2, 3) | | Typ | TBD | | | | µs |
| | | Effective Write Buffer Program Operation (Notes 2, 4) | Per Word | Typ | TBD | | | | µs |
| | | Accelerated Effective Write Buffer Program Operation (Notes 2, 4) | Per Word | Typ | TBD | | | | µs |
| | | Program Operation (Note 2) | Word | Typ | TBD | | | | µs |
| | | Accelerated Programming Operation (Note 2) | Word | Typ | TBD | | | | µs |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Note 2) | | Typ | TBD | | | | sec |
| | $t_{VHH}$ | $V_{HH}$ Rise and Fall Time (Note 1) | | Min | 250 | | | | ns |
| | $t_{VCS}$ | $V_{CC}$ Setup Time (Note 1) | | Min | 50 | | | | µs |

***Notes:***

1. *Not 100% tested.*
2. *See the "AC Characteristics" section for more information.*
3. *For 1–16 words/1–32 bytes programmed.*
4. *Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.*
5. *Unless otherwise indicated, AC specifications for 80 ns and 90 ns speed options are tested with $V_{IO} = V_{CC} = 3$ V. AC specifications for 90 ns and 100 ns speed options are tested with $V_{IO} = 1.8$ V and $V_{CC} = 3.0$ V.*

# AC Characteristics

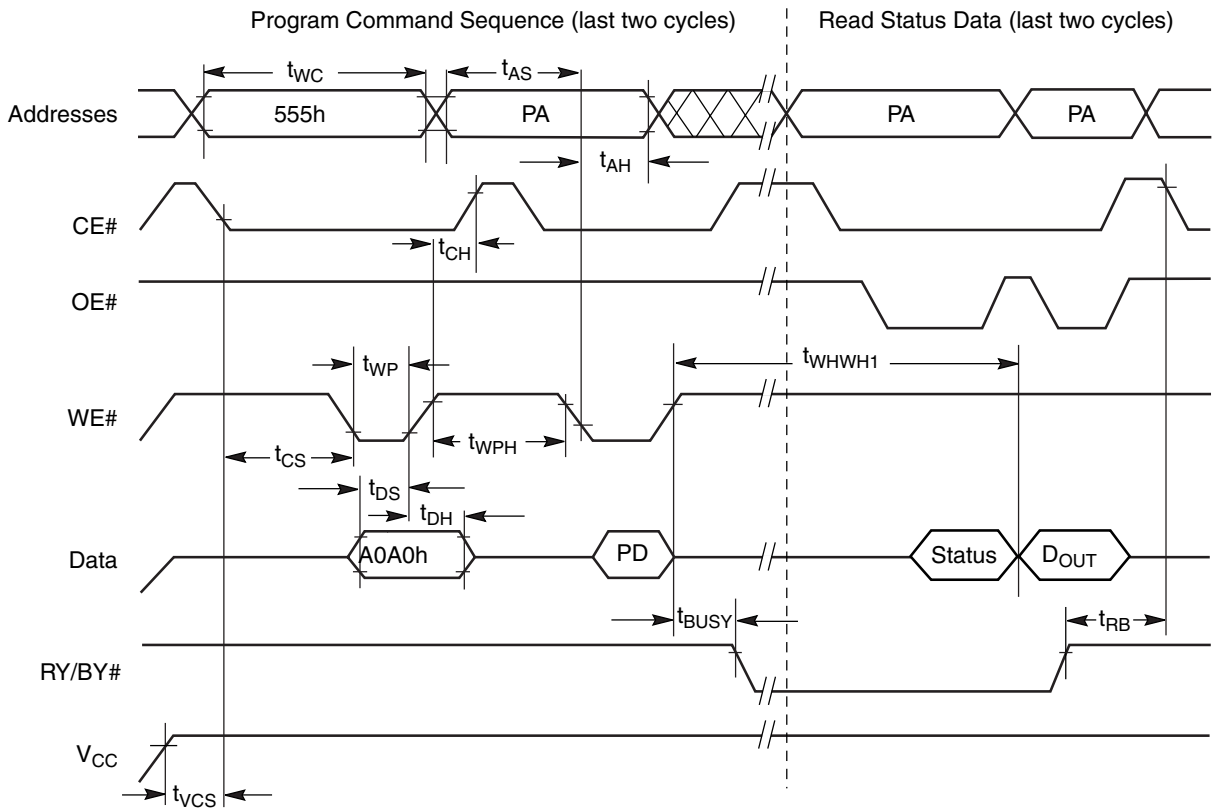
## Erase and Program Operations–S29GLI28N Only

| Parameter | | Description | | | Speed Options | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Std. | | | | 80 | 90 | 90 | 100 | |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time (Note 1) | | Min | 80 | 90 | 90 | 100 | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Setup Time | | Min | 0 | | | | ns |
| | $t_{ASO}$ | Address Setup Time to OE# low during toggle bit polling | | Min | 15 | | | | ns |
| $t_{WLAX}$ | $t_{AH}$ | Address Hold Time | | Min | 45 | | | | ns |
| | $t_{AHT}$ | Address Hold Time From CE# or OE# high during toggle bit polling | | Min | 0 | | | | ns |
| $t_{DVWH}$ | $t_{DS}$ | Data Setup Time | | Min | 45 | | | | ns |
| $t_{WHDX}$ | $t_{DH}$ | Data Hold Time | | Min | 0 | | | | ns |
| | $t_{OEPH}$ | Output Enable High during toggle bit polling | | Min | 20 | | | | ns |
| $t_{GHWL}$ | $t_{GHWL}$ | Read Recovery Time Before Write (OE# High to WE# Low) | | Min | 0 | | | | ns |
| $t_{ELWL}$ | $t_{CS}$ | CE# Setup Time | | Min | 0 | | | | ns |
| $t_{WHEH}$ | $t_{CH}$ | CE# Hold Time | | Min | 0 | | | | ns |
| $t_{WLWH}$ | $t_{WP}$ | Write Pulse Width | | Min | 35 | | | | ns |
| $t_{WHDL}$ | $t_{WPH}$ | Write Pulse Width High | | Min | 30 | | | | ns |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Write Buffer Program Operation (Notes 2, 3) | | Typ | TBD | | | | µs |
| | | Effective Write Buffer Program Operation (Notes 2, 4) | Per Word | Typ | TBD | | | | µs |
| | | Accelerated Effective Write Buffer Program Operation (Notes 2, 4) | Per Word | Typ | TBD | | | | µs |
| | | Program Operation (Note 2) | Word | Typ | TBD | | | | µs |
| | | Accelerated Programming Operation (Note 2) | Word | Typ | TBD | | | | µs |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Note 2) | | Typ | TBD | | | | sec |
| | $t_{VHH}$ | $V_{HH}$ Rise and Fall Time (Note 1) | | Min | 250 | | | | ns |
| | $t_{VCS}$ | $V_{CC}$ Setup Time (Note 1) | | Min | 50 | | | | µs |

***Notes:***

1. *Not 100% tested.*
2. *See the "AC Characteristics" section for more information.*
3. *For 1–16 words/1–32 bytes programmed.*
4. *Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.*
5. *Unless otherwise indicated, AC specifications for 80 ns and 90 ns speed options are tested with $V_{IO} = V_{CC} = 3$ V. AC specifications for 90 ns and 100 ns speed options are tested with $V_{IO} = 1.8$ V and $V_{CC} = 3.0$ V.*

## AC Characteristics




***Notes:***

1. *PA = program address, PD = program data, $D_{OUT}$ is the true data at the program address.*
2. *Illustration shows device in word mode.*

**Figure 14. Program Operation Timings**

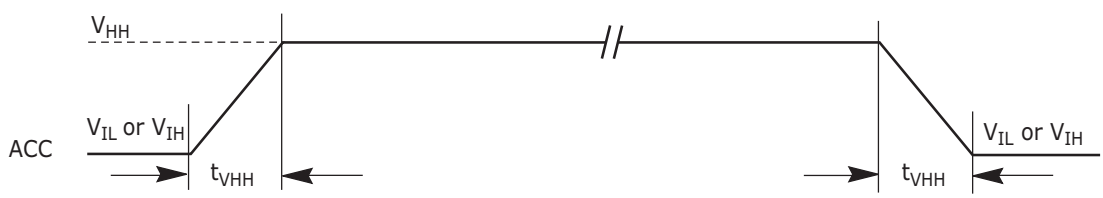
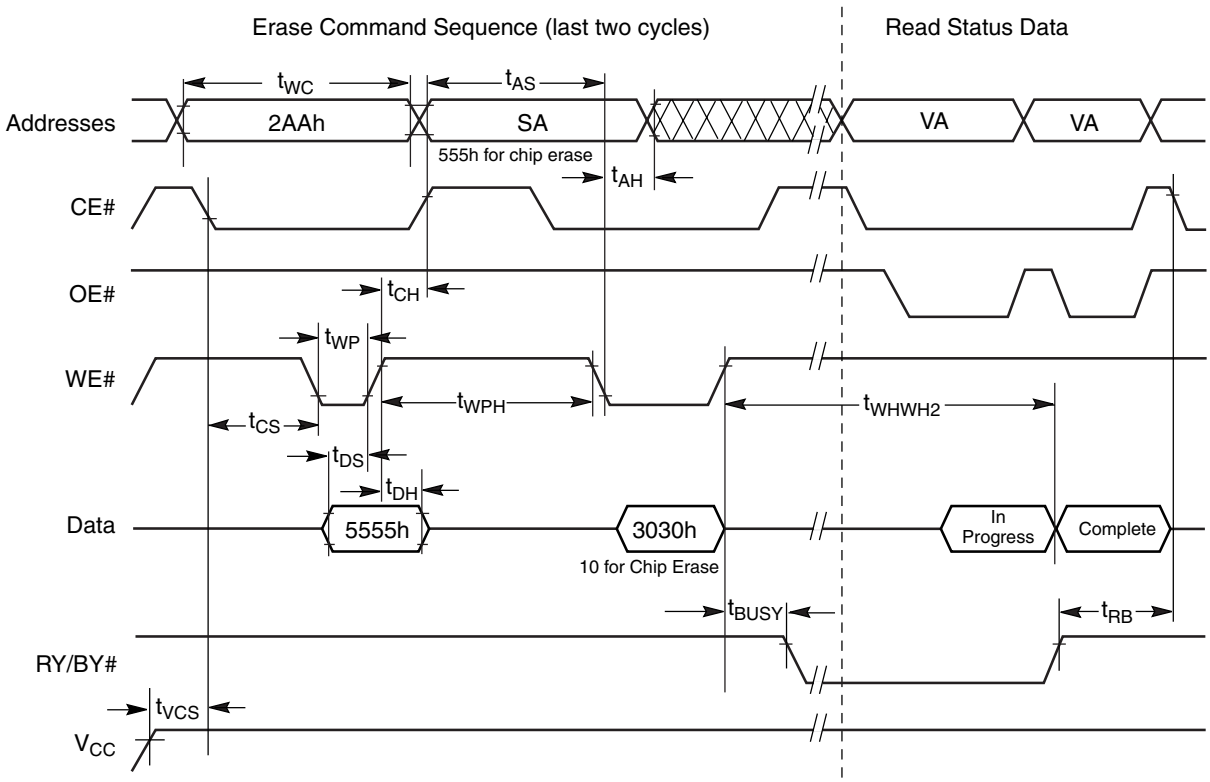



**Figure 15. Accelerated Program Timing Diagram**

***Notes:***

1. *Not 100% tested.*
2. *CE#, OE# = $V_{IL}$*
3. *OE# = $V_{IL}$*
4. *See Figure 9 and Table 13 for test specifications.*

## AC Characteristics

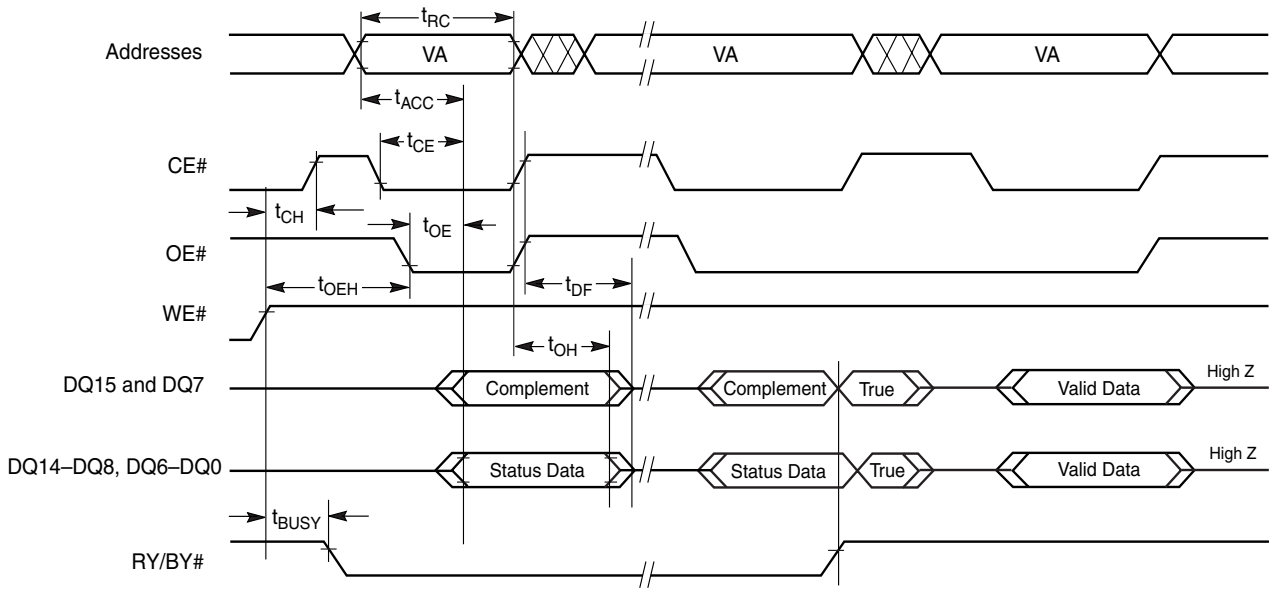



***Notes:***

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status".*
2. *These waveforms are for the word mode.*

**Figure 16. Chip/Sector Erase Operation Timings**

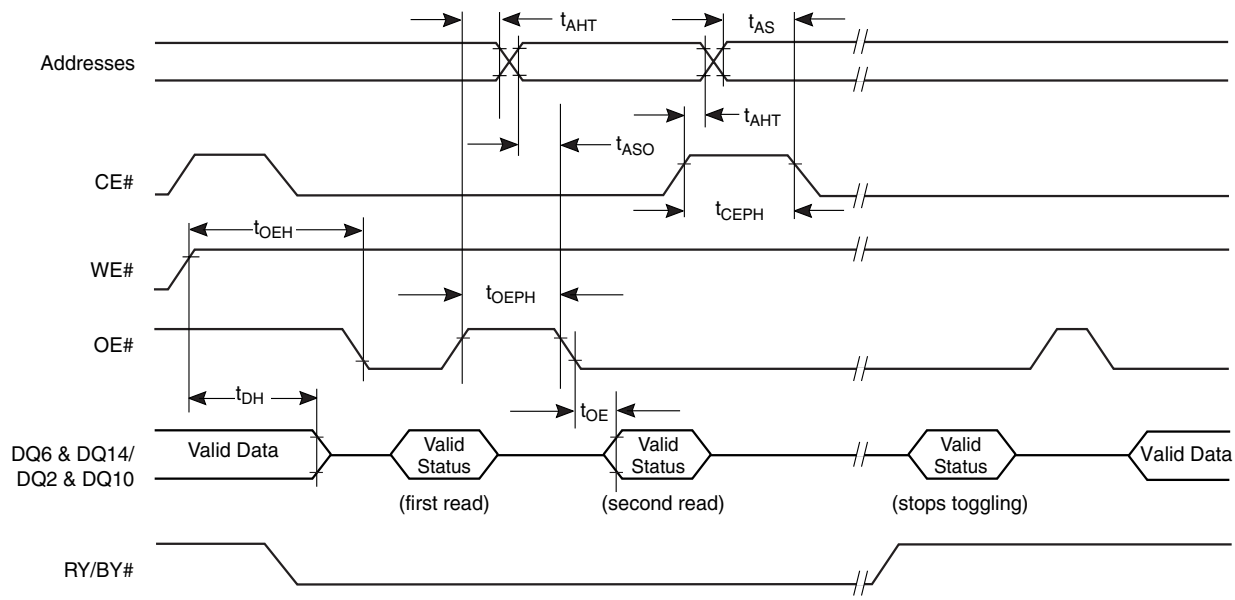
## AC Characteristics




***Note:*** *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

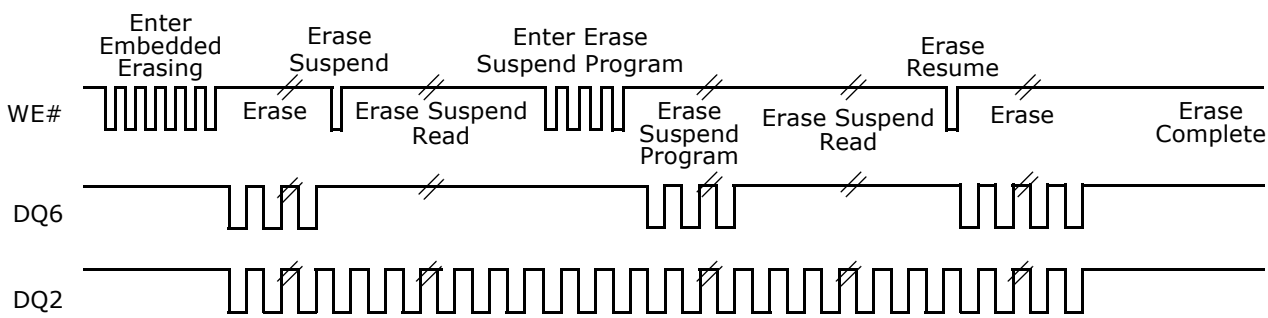
**Figure 17. Data# Polling Timings (During Embedded Algorithms)**

## AC Characteristics




***Note:*** *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle*

**Figure 18. Toggle Bit Timings (During Embedded Algorithms)**




***Note:*** *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.*

**Figure 19. DQ2 vs. DQ6**

# AC Characteristics

## Alternate CE# Controlled Erase and Program Operations–S29GL5I2N Only

| Parameter | | Description | | | Speed Options | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Std. | | | | 90 | 100 | 100 | 110 | |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time (Note 1) | | Min | 90 | 100 | 100 | 110 | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Setup Time | | Min | 0 | | | | ns |
| $t_{ELAX}$ | $t_{AH}$ | Address Hold Time | | Min | 45 | | | | ns |
| $t_{DVEH}$ | $t_{DS}$ | Data Setup Time | | Min | 45 | | | | ns |
| $t_{EHDX}$ | $t_{DH}$ | Data Hold Time | | Min | 0 | | | | ns |
| $t_{GHEL}$ | $t_{GHEL}$ | Read Recovery Time Before Write (OE# High to WE# Low) | | Min | 0 | | | | ns |
| $t_{WLEL}$ | $t_{WS}$ | WE# Setup Time | | Min | 0 | | | | ns |
| $t_{EHWH}$ | $t_{WH}$ | WE# Hold Time | | Min | 0 | | | | ns |
| $t_{ELEH}$ | $t_{CP}$ | CE# Pulse Width | | Min | 45 | | | | ns |
| $t_{EHEL}$ | $t_{CPH}$ | CE# Pulse Width High | | Min | 30 | | | | ns |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Write Buffer Program Operation (Notes 2, 3) | | Typ | TBD | | | | µs |
| | | Effective Write Buffer Program Operation (Notes 2, 4) | Per Word | Typ | TBD | | | | µs |
| | | Effective Accelerated Write Buffer Program Operation (Notes 2, 4) | Per Word | Typ | TBD | | | | µs |
| | | Program Operation (Note 2) | Word | Typ | TBD | | | | µs |
| | | Accelerated Programming Operation (Note 2) | Word | Typ | TBD | | | | µs |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Note 2) | | Typ | TBD | | | | sec |

***Notes:***

1. *Not 100% tested.*
2. *See the "AC Characteristics" section for more information.*
3. *For 1–16 words/1–32 bytes programmed.*
4. *Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.*
5. *Unless otherwise indicated, AC specifications for 90 ns and 100 ns speed options are tested with $V_{IO}$ = $V_{CC}$ = 3 V. AC specifications for 100 ns and 110 ns speed options are tested with $V_{IO}$ = 1.8 V and $V_{CC}$ = 3.0 V.*

# AC Characteristics

## Alternate CE# Controlled Erase and Program Operations–S29GL256N Only

| Parameter | | Description | | | Speed Options | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Std. | | | | 80 | 90 | 90 | 100 | |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time (Note 1) | | Min | 80 | 90 | 90 | 100 | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Setup Time | | Min | 0 | | | | ns |
| $t_{ELAX}$ | $t_{AH}$ | Address Hold Time | | Min | 45 | | | | ns |
| $t_{DVEH}$ | $t_{DS}$ | Data Setup Time | | Min | 45 | | | | ns |
| $t_{EHDX}$ | $t_{DH}$ | Data Hold Time | | Min | 0 | | | | ns |
| $t_{GHEL}$ | $t_{GHEL}$ | Read Recovery Time Before Write (OE# High to WE# Low) | | Min | 0 | | | | ns |
| $t_{WLEL}$ | $t_{WS}$ | WE# Setup Time | | Min | 0 | | | | ns |
| $t_{EHWH}$ | $t_{WH}$ | WE# Hold Time | | Min | 0 | | | | ns |
| $t_{ELEH}$ | $t_{CP}$ | CE# Pulse Width | | Min | 45 | | | | ns |
| $t_{EHEL}$ | $t_{CPH}$ | CE# Pulse Width High | | Min | 30 | | | | ns |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Write Buffer Program Operation (Notes 2, 3) | | Typ | TBD | | | | µs |
| | | Effective Write Buffer Program Operation (Notes 2, 4) | Per Word | Typ | TBD | | | | µs |
| | | Effective Accelerated Write Buffer Program Operation (Notes 2, 4) | Per Word | Typ | TBD | | | | µs |
| | | Program Operation (Note 2) | Word | Typ | TBD | | | | µs |
| | | Accelerated Programming Operation (Note 2) | Word | Typ | TBD | | | | µs |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Note 2) | | Typ | TBD | | | | sec |

***Notes:***

1. *Not 100% tested.*
2. *See the "AC Characteristics" section for more information.*
3. *For 1–16 words/1–32 bytes programmed.*
4. *Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.*
5. *Unless otherwise indicated, AC specifications for 80 ns and 90 ns speed options are tested with $V_{IO} = V_{CC} = 3$ V. AC specifications for 90 ns and 100 ns speed options are tested with $V_{IO} = 1.8$ V and $V_{CC} = 3.0$ V.*

# AC Characteristics

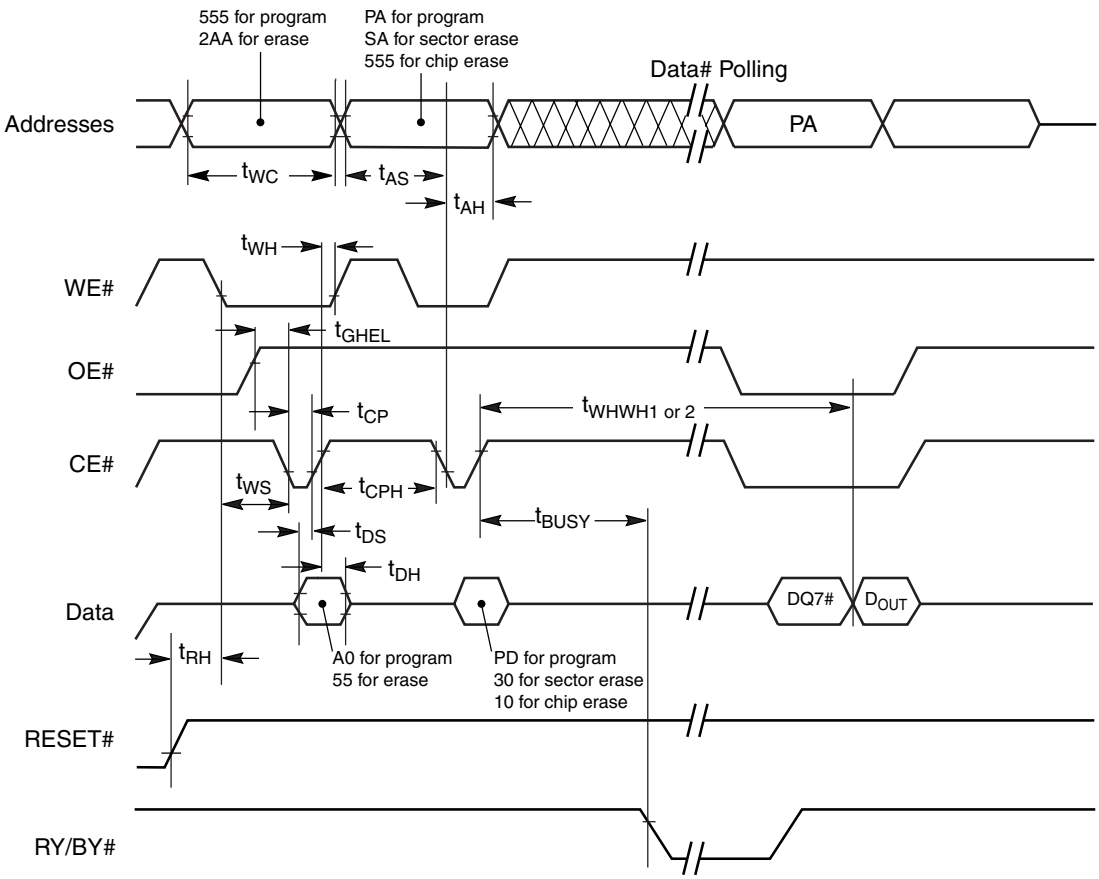
## Alternate CE# Controlled Erase and Program Operations–S29GLI28N Only

| Parameter | | Description | | | Speed Options | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Std. | | | | 80 | 90 | 90 | 100 | |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time (Note 1) | | Min | 80 | 90 | 90 | 100 | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Setup Time | | Min | 0 | | | | ns |
| $t_{ELAX}$ | $t_{AH}$ | Address Hold Time | | Min | 45 | | | | ns |
| $t_{DVEH}$ | $t_{DS}$ | Data Setup Time | | Min | 45 | | | | ns |
| $t_{EHDX}$ | $t_{DH}$ | Data Hold Time | | Min | 0 | | | | ns |
| $t_{GHEL}$ | $t_{GHEL}$ | Read Recovery Time Before Write (OE# High to WE# Low) | | Min | 0 | | | | ns |
| $t_{WLEL}$ | $t_{WS}$ | WE# Setup Time | | Min | 0 | | | | ns |
| $t_{EHWH}$ | $t_{WH}$ | WE# Hold Time | | Min | 0 | | | | ns |
| $t_{ELEH}$ | $t_{CP}$ | CE# Pulse Width | | Min | 45 | | | | ns |
| $t_{EHEL}$ | $t_{CPH}$ | CE# Pulse Width High | | Min | 30 | | | | ns |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Write Buffer Program Operation (Notes 2, 3) | | Typ | TBD | | | | µs |
| | | Effective Write Buffer Program Operation (Notes 2, 4) | Per Word | Typ | TBD | | | | µs |
| | | Effective Accelerated Write Buffer Program Operation (Notes 2, 4) | Per Word | Typ | TBD | | | | µs |
| | | Program Operation (Note 2) | Word | Typ | TBD | | | | µs |
| | | Accelerated Programming Operation (Note 2) | Word | Typ | TBD | | | | µs |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Note 2) | | Typ | TBD | | | | sec |

***Notes:***

1. *Not 100% tested.*
2. *See the "AC Characteristics" section for more information.*
3. *For 1–16 words/1–32 bytes programmed.*
4. *Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.*
5. *Unless otherwise indicated, AC specifications for 80 ns and 90 ns speed options are tested with $V_{IO} = V_{CC} = 3$ V. AC specifications for 90 ns and 100 ns speed options are tested with $V_{IO} = 1.8$ V and $V_{CC} = 3.0$ V.*

## AC Characteristics




***Notes:***

1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. $D_{OUT}$ is the data written to the device.*
4. *Waveforms are for the word mode.*

**Figure 20. Alternate CE# Controlled Write (Erase/Program) Operation Timings**

## Latchup Characteristics

| Description | Min | Max |
|---|---|---|
| Input voltage with respect to $V_{SS}$ on all pins except I/O pins (including A9, OE#, and RESET#) | −1.0 V | 12.5 V |
| Input voltage with respect to $V_{SS}$ on all I/O pins | −1.0 V | $V_{CC}$ + 1.0 V |
| $V_{CC}$ Current | −100 mA | +100 mA |

***Note:*** *Includes all pins except $V_{CC}$. Test conditions: $V_{CC}$ = 3.0 V, one pin at a time.*

## Erase And Programming Performance

| Parameter | | Typ (Note 1) | Max (Note 2) | Unit | Comments |
|---|---|---|---|---|---|
| Sector Erase Time | | TBD | TBD | sec | Excludes 00h programming prior to erasure (Note 5) |
| Chip Erase Time | S29GL128N | TBD | TBD | sec | |
| | S29GL256N | TBD | TBD | | |
| | S29GL512N | TBD | TBD | | |
| Total Write Buffer Time (Note 3) | | TBD | TBD | µs | Excludes system level overhead (Note 6) |
| Total Accelerated Effective Write Buffer Programming Time (Note 3) | | TBD | TBD | µs | |
| Chip Program Time | S29GL128N | TBD | TBD | sec | |
| | S29GL256N | TBD | TBD | | |
| | S29GL512N | TBD | TBD | | |

***Notes:***

1. *Typical program and erase times assume the following conditions: 10,000 cycles, 25°C, 3.0 V $V_{CC}$, checkerboard pattern.*
2. *Under worst case conditions of 100,000 cycles, 90°C, $V_{CC}$ = 3.0 V.*
3. *Effective write buffer specification is based upon a 16-word write buffer operation.*
4. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most words program faster than the maximum program times listed.*
5. *In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.*
6. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 17 for further information on command definitions.*

## TSOP Pin and BGA Package Capacitance

| Parameter Symbol | Parameter Description | Test Setup | | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 | TSOP | 6 | 7.5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 | TSOP | 8.5 | 12 | pF |
| $C_{IN2}$ | Control Pin Capacitance | $V_{IN}$ = 0 | TSOP | 7.5 | 9 | pF |

***Notes:***

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A$ = 25°C, f = 1.0 MHz.*

# pSRAM Type I

## 4Mbit (256K Word x 16-bit)
## 8Mbit (512K Word x 16-bit)
## 16Mbit (1M Word x 16-bit)
## 32Mbit (2M Word x 16-bit)
## 64Mbit (4M Word x 16-bit)

## Functional Description

| Mode | CE# | CE2/ZZ# | OE# | WE# | UB# | LB# | Addresses | I/O 1-8 | I/O 9-16 | Power |
|---|---|---|---|---|---|---|---|---|---|---|
| Read (word) | L | H | L | H | L | L | X | Dout | Dout | $I_{ACTIVE}$ |
| Read (lower byte) | L | H | L | H | H | L | X | Dout | High-Z | $I_{ACTIVE}$ |
| Read (upper byte) | L | H | L | H | L | H | X | High-Z | Dout | $I_{ACTIVE}$ |
| Write (word) | L | H | X | L | L | L | X | Din | Din | $I_{ACTIVE}$ |
| Write (lower byte) | L | H | X | L | H | L | X | Din | Invalid | $I_{ACTIVE}$ |
| Write (upper byte) | L | H | X | L | L | H | X | Invalid | Din | $I_{ACTIVE}$ |
| Outputs disabled | L | H | H | H | X | X | X | High-Z | High-Z | $I_{ACTIVE}$ |
| Standby | H | H | X | X | X | X | X | High-Z | High-Z | $I_{STANDBY}$ |
| Deep power down | H | L | X | X | X | X | X | High-Z | High-Z | $I_{DEEP\ SLEEP}$ |

## Absolute Maximum Ratings

| Item | Symbol | Ratings | Units |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | Vin, Vout | -0.2 to $V_{CC}$ +0.3 | V |
| Voltage on $V_{CC}$ relative to $V_{SS}$ | $V_{CC}$ | -0.2 to 3.6 | V |
| Power dissipation | $P_D$ | 1 | W |
| Storage temperature | $T_{STG}$ | -55 to 150 | °C |
| Operating temperature | $T_A$ | -25 to 85 | °C |

# DC Characteristics (4Mb pSRAM Asynchronous)

| | | | Asynchronous | | |
|---|---|---|---|---|---|
| | | **Performance Grade** | **-70** | | |
| | | **Density** | **4Mb pSRAM** | | |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Units** |
| $V_{CC}$ | Power Supply | | 2.7 | 3.3 | V |
| $V_{IH}$ | Input High Level | | 0.8 Vccq | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Level | | -0.3 | 0.4 | V |
| $I_{IL}$ | Input Leakage Current | Vin = 0 to $V_{CC}$ | | 0.5 | µA |
| $I_{LO}$ | Output Leakage Current | OE = $V_{IH}$ or Chip Disabled | | 0.5 | µA |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -1.0 mA | | | V |
| | | $I_{OH}$ = -0.2 mA | 0.8 Vccq | | |
| | | $I_{OH}$ = -0.5 mA | | | |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.0 mA | | | V |
| | | $I_{OL}$ = 0.2 mA | | 0.2 | |
| | | $I_{OL}$ = 0.5 mA | | | |
| $I_{ACTIVE}$ | Operating Current | $V_{CC}$ = 3.3 V | | 25 | mA |
| $I_{STANDBY}$ | Standby Current | $V_{CC}$ = 3.0 V | | 70 | µA |
| | | $V_{CC}$ = 3.3 V | | | |
| $I_{DEEP\ SLEEP}$ | Deep Power Down Current | | | x | µA |
| $I_{PAR\ 1/4}$ | 1/4 Array PAR Current | | | x | µA |
| $I_{PAR\ 1/2}$ | 1/2 Array PAR Current | | | x | µA |

# DC Characteristics (8Mb pSRAM Asynchronous)

| | | | Asynchronous | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Version** | | | **B** | | | | | | **C** | | |
| **Performance Grade** | | | **-55** | | | **-70** | | | **-70** | | |
| **Density** | | | **8Mb pSRAM** | | | **8Mb pSRAM** | | | **8Mb pSRAM** | | |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Units** | **Min** | **Max** | **Units** | **Min** | **Max** | **Units** |
| $V_{CC}$ | Power Supply | | 2.7 | 3.3 | V | 2.7 | 3.6 | V | 2.7 | 3.3 | V |
| $V_{IH}$ | Input High Level | | 2.2 | $V_{CC}$ + 0.3 | V | 2.2 | $V_{CC}$ + 0.3 | V | 0.8 | $V_{CC}$+0.3 | V |
| $V_{IL}$ | Input Low Level | | -0.3 | 0.6 | V | -0.3 | 0.6 | V | -0.3 | 0.4 | V |
| $I_{IL}$ | Input Leakage Current | Vin = 0 to $V_{CC}$ | | 0.5 | µA | | 0.5 | µA | | 0.5 | µA |
| $I_{LO}$ | Output Leakage Current | OE = $V_{IH}$ or Chip Disabled | | 0.5 | µA | | 0.5 | µA | | 0.5 | µA |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -1.0 mA | $V_{CC}$-0.4 | | V | $V_{CC}$-0.4 | | V | | | V |
| | | $I_{OH}$ = -0.2 mA | | | | | | | 0.8 $V_{CCQ}$ | | |
| | | $I_{OH}$ = -0.5 mA | | | | | | | | | |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.0 mA | | 0.4 | V | | 0.4 | V | | | V |
| | | $I_{OL}$ = 0.2 mA | | | | | | | | 0.2 | |
| | | $I_{OL}$ = 0.5 mA | | | | | | | | | |
| $I_{ACTIVE}$ | Operating Current | $V_{CC}$ = 3.3 V | | 25 | mA | | 23 | mA | | 25 | mA |
| $I_{STANDBY}$ | Standby Current | $V_{CC}$ = 3.0 V | | 60 | µA | | 60 | µA | | 70 | µA |
| | | $V_{CC}$ = 3.3 V | | | | | | | | | |
| $I_{DEEP\ SLEEP}$ | Deep Power Down Current | | | x | µA | | x | µA | | x | µA |
| $I_{PAR\ 1/4}$ | 1/4 Array PAR Current | | | x | µA | | x | µA | | x | µA |
| $I_{PAR\ 1/2}$ | 1/2 Array PAR Current | | | x | µA | | x | µA | | x | µA |

# DC Characteristics (16Mb pSRAM Asynchronous)

| | | | Asynchronous | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | Performance Grade | -55 | | | -70 | | |
| | | Density | 16Mb pSRAM | | | 16Mb pSRAM | | |
| **Symbol** | **Parameter** | **Conditions** | **Minimum** | **Maximum** | **Units** | **Minimum** | **Maximum** | **Units** |
| $V_{CC}$ | Power Supply | | 2.7 | 3.6 | V | 2.7 | 3.6 | V |
| $V_{IH}$ | Input High Level | | 2.2 | $V_{CC}$ + 0.3 | V | 2.2 | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Level | | -0.3 | 0.6 | V | -0.3 | 0.6 | V |
| $I_{IL}$ | Input Leakage Current | Vin = 0 to $V_{CC}$ | | 0.5 | µA | | 0.5 | µA |
| $I_{LO}$ | Output Leakage Current | OE = $V_{IH}$ or Chip Disabled | | 0.5 | µA | | 0.5 | µA |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -1.0 mA | $V_{CC}$-0.4 | | V | $V_{CC}$-0.4 | | V |
| | | $I_{OH}$ = -0.2 mA | | | | | | |
| | | $I_{OH}$ = -0.5 mA | | | | | | |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.0 mA | | 0.4 | V | | 0.4 | V |
| | | $I_{OL}$ = 0.2 mA | | | | | | |
| | | $I_{OL}$ = 0.5 mA | | | | | | |
| $I_{ACTIVE}$ | Operating Current | $V_{CC}$ = 3.3 V | | 25 | mA | | 25 | mA |
| $I_{STANDBY}$ | Standby Current | $V_{CC}$ = 3.0 V | | 100 | µA | | 100 | µA |
| | | $V_{CC}$ = 3.3 V | | | | | | |
| $I_{DEEP\ SLEEP}$ | Deep Power Down Current | | | x | µA | | x | µA |
| $I_{PAR\ 1/4}$ | 1/4 Array PAR Current | | | x | µA | | x | µA |
| $I_{PAR\ 1/2}$ | 1/2 Array PAR Current | | | x | µA | | x | µA |

# DC Characteristics (16Mb pSRAM Page Mode)

| | | | Page Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Performance Grade** | | | **-60** | | | **-65** | | | **-70** | | |
| **Density** | | | **16Mb pSRAM** | | | **16Mb pSRAM** | | | **16Mb pSRAM** | | |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Units** | **Min** | **Max** | **Units** | **Min** | **Max** | **Units** |
| $V_{CC}$ | Power Supply | | 2.7 | 3.3 | V | 2.7 | 3.3 | V | 2.7 | 3.3 | V |
| $V_{IH}$ | Input High Level | | 0.8 Vccq | $V_{CC}$ + 0.2 | V | 0.8 Vccq | $V_{CC}$ + 0.2 | V | 0.8 Vccq | $V_{CC}$ + 0.2 | V |
| $V_{IL}$ | Input Low Level | | -0.2 | 0.2 Vccq | V | -0.2 | 0.2 Vccq | V | -0.2 | 0.2 Vccq | V |
| $I_{IL}$ | Input Leakage Current | Vin = 0 to $V_{CC}$ | | 1 | µA | | 1 | µA | | 1 | µA |
| $I_{LO}$ | Output Leakage Current | OE = $V_{IH}$ or Chip Disabled | | 1 | µA | | 1 | µA | | 1 | µA |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -1.0 mA | | | V | | | V | | | V |
| | | $I_{OH}$ = -0.2 mA | | | | | | | | | |
| | | $I_{OH}$ = -0.5 mA | 0.8 Vccq | | | 0.8 Vccq | | | 0.8 Vccq | | |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.0 mA | | | V | | | V | | | V |
| | | $I_{OL}$ = 0.2 mA | | | | | | | | | |
| | | $I_{OL}$ = 0.5 mA | | 0.2 Vccq | | | 0.2 Vccq | | | 0.2 Vccq | |
| $I_{ACTIVE}$ | Operating Current | $V_{CC}$ = 3.3 V | | 25 | mA | | 25 | mA | | 25 | mA |
| $I_{STANDBY}$ | Standby Current | $V_{CC}$ = 3.0 V | | | µA | | | µA | | | µA |
| | | $V_{CC}$ = 3.3 V | | 100 | | | 100 | | | 100 | |
| $I_{DEEP\ SLEEP}$ | Deep Power Down Current | | | 10 | µA | | 10 | µA | | 10 | µA |
| $I_{PAR\ 1/4}$ | 1/4 Array PAR Current | | | 65 | µA | | 65 | µA | | 65 | µA |
| $I_{PAR\ 1/2}$ | 1/2 Array PAR Current | | | 80 | µA | | 80 | µA | | 80 | µA |

# DC Characteristics (32Mb pSRAM Page Mode)

| | | | Page Mode | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Version** | | | **C** | | | **E** | | | | | | | | |
| **Performance Grade** | | | **-65** | | | **-60** | | | **-65** | | | **-70** | | |
| **Density** | | | **32Mb pSRAM** | | | **32Mb pSRAM** | | | **32Mb pSRAM** | | | **32Mb pSRAM** | | |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Units** | **Min** | **Max** | **Units** | **Min** | **Max** | **Units** | **Min** | **Max** | **Units** |
| $V_{CC}$ | Power Supply | | 2.7 | 3.6 | V | 2.7 | 3.3 | V | 2.7 | 3.3 | V | 2.7 | 3.3 | V |
| $V_{IH}$ | Input High Level | | 1.4 | $V_{CC}$ + 0.2 | V | 0.8 Vccq | $V_{CC}$ + 0.2 | V | 0.8 Vccq | $V_{CC}$ + 0.2 | V | 0.8 Vccq | $V_{CC}$ + 0.2 | V |
| $V_{IL}$ | Input Low Level | | -0.2 | 0.4 | V | -0.2 | 0.2 Vccq | V | -0.2 | 0.2 Vccq | V | -0.2 | 0.2 Vccq | V |
| $I_{IL}$ | Input Leakage Current | Vin = 0 to $V_{CC}$ | | 0.5 | µA | | 1 | µA | | 1 | µA | | 1 | µA |
| $I_{LO}$ | Output Leakage Current | OE = $V_{IH}$ or Chip Disabled | | 0.5 | µA | | 1 | µA | | 1 | µA | | 1 | µA |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -1.0 mA | | | V | | | V | | | V | | | V |
| | | $I_{OH}$ = -0.2 mA | 0.8 Vccq | | | | | | | | | | | |
| | | $I_{OH}$ = -0.5 mA | | | | 0.8 Vccq | | | 0.8 Vccq | | | 0.8 Vccq | | |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.0 mA | | | V | | | V | | | V | | | V |
| | | $I_{OL}$ = 0.2 mA | | 0.2 | | | | | | | | | | |
| | | $I_{OL}$ = 0.5 mA | | | | | 0.2 Vccq | | | 0.2 Vccq | | | 0.2 Vccq | |
| $I_{ACTIVE}$ | Operating Current | $V_{CC}$ = 3.3 V | | 25 | mA | | 25 | mA | | 25 | mA | | 25 | mA |
| $I_{STANDBY}$ | Standby Current | $V_{CC}$ = 3.0 V | | | µA | | | µA | | | µA | | | µA |
| | | $V_{CC}$ = 3.3 V | | 100 | | | 120 | | | 120 | | | 120 | |
| $I_{DEEP\ SLEEP}$ | Deep Power Down Current | | | 10 | µA | | 10 | µA | | 10 | µA | | 10 | µA |
| $I_{PAR\ 1/4}$ | 1/4 Array PAR Current | | | 65 | µA | | 75 | µA | | 75 | µA | | 75 | µA |
| $I_{PAR\ 1/2}$ | 1/2 Array PAR Current | | | 80 | µA | | 90 | µA | | 90 | µA | | 90 | µA |

## DC Characteristics (64Mb pSRAM Page Mode)

| | | | Page Mode | | |
|---|---|---|---|---|---|
| Performance Grade | | | -70 | | |
| Density | | | 64Mb pSRAM | | |
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Units** |
| $V_{CC}$ | Power Supply | | 2.7 | 3.3 | V |
| $V_{IH}$ | Input High Level | | 0.8 Vccq | $V_{CC}$ + 0.2 | V |
| $V_{IL}$ | Input Low Level | | -0.2 | 0.2 Vccq | V |
| $I_{IL}$ | Input Leakage Current | Vin = 0 to $V_{CC}$ | | 1 | µA |
| $I_{LO}$ | Output Leakage Current | OE = $V_{IH}$ or Chip Disabled | | 1 | µA |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -1.0 mA | | | V |
| | | $I_{OH}$ = -0.2 mA | | | |
| | | $I_{OH}$ = -0.5 mA | 0.8 Vccq | | |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.0 mA | | | V |
| | | $I_{OL}$ = 0.2 mA | | | |
| | | $I_{OL}$ = 0.5 mA | | 0.2 Vccq | |
| $I_{ACTIVE}$ | Operating Current | $V_{CC}$ = 3.3 V | | 25 | mA |
| $I_{STANDBY}$ | Standby Current | $V_{CC}$ = 3.0 V | | | µA |
| | | $V_{CC}$ = 3.3 V | | 120 | |
| $I_{DEEP\ SLEEP}$ | Deep Power Down Current | | | 10 | µA |
| $I_{PAR\ 1/4}$ | 1/4 Array PAR Current | | | 65 | µA |
| $I_{PAR\ 1/2}$ | 1/2 Array PAR Current | | | 80 | µA |

## Timing Test Conditions

| Item | |
|---|---|
| Input Pulse Level | 0.1 $V_{CC}$ to 0.9 $V_{CC}$ |
| Input Rise and Fall Time | 5ns |
| Input and Output Timing Reference Levels | 0.5 $V_{CC}$ |
| Operating Temperature | -25°C to +85°C |

### Output Load Circuit

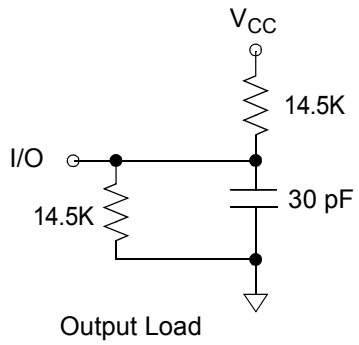



**Figure 21. Output Load Circuit**

## Power Up Sequence

After applying power, maintain a stable power supply for a minimum of 200 µs after CE# > $V_{IH}$.

# AC Characteristics

## (4Mb pSRAM Page Mode)

| | | | Asynchronous | | |
|---|---|---|---|---|---|
| | | Performance Grade | -70 | | |
| | | Density | 4Mb pSRAM | | |
| 3 Volt | Symbol | Parameter | Min | Max | Units |
| Read | trc | Read cycle time | 70 | | ns |
| | taa | Address Access Time | | 70 | ns |
| | tco | Chip select to output | | 70 | ns |
| | toe | Output enable to valid output | | 20 | ns |
| | tba | UB#, LB# Access time | | 70 | ns |
| | tlz | Chip select to Low-z output | 10 | | ns |
| | tblz | UB#, LB# Enable to Low-Z output | 10 | | ns |
| | tolz | Output enable to Low-Z output | 5 | | ns |
| | thz | Chip enable to High-Z output | 0 | 20 | ns |
| | tbhz | UB#, LB# disable to High-Z output | 0 | 20 | ns |
| | tohz | Output disable to High-Z output | 0 | 20 | ns |
| | toh | Output hold from Address Change | 10 | | ns |

| | | | Asynchronous | | |
|---|---|---|---|---|---|
| | | Performance Grade | -70 | | |
| | | Density | 4Mb pSRAM | | |
| 3 Volt | Symbol | Parameter | Min | Max | Units |
| Write | twc | Write cycle time | 70 | | ns |
| | tcw | Chipselect to end of write | 70 | | ns |
| | tas | Address set up Time | 0 | | ns |
| | taw | Address valid to end of write | 70 | | ns |
| | tbw | UB#, LB# valid to end of write | 70 | | ns |
| | twp | Write pulse width | 55 | | ns |
| | twr | Write recovery time | 0 | | ns |
| | twhz | Write to output High-Z | | 20 | ns |
| | tdw | Data to write time overlap | 25 | | ns |
| | tdh | Data hold from write time | 0 | | ns |
| | tow | End write to output Low-Z | 5 | | |
| | tow | Write high pulse width | 7.5 | | ns |
| | | | | | |
| Other | tpc | Page read cycle | x | | |
| | tpa | Page address access time | | x | |
| | twpc | Page write cycle | x | | |
| | tcp | Chip select high pulse width | x | | |

# AC Characteristics

## (8Mb pSRAM Asynchronous)

| | | | Asynchronous | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Version | B | | | | | | C | | |
| | | Performance Grade | -55 | | | -70 | | | -70 | | |
| | | Density | 8Mb pSRAM | | | 8Mb pSRAM | | | 8Mb pSRAM | | |
| 3 Volt | Symbol | Parameter | Min | Max | Units | Min | Max | Units | Min | Max | Units |
| Read | trc | Read cycle time | 55 | | ns | 70 | | ns | 70 | | ns |
| | taa | Address Access Time | | 55 | ns | | 70 | ns | | 70 | ns |
| | tco | Chip select to output | | 55 | ns | | 70 | ns | | 70 | ns |
| | toe | Output enable to valid output | | 30 | ns | | 35 | ns | | 20 | ns |
| | tba | UB#, LB# Access time | | 55 | ns | | 70 | ns | | 70 | ns |
| | tlz | Chip select to Low-z output | 5 | | ns | 5 | | ns | 10 | | ns |
| | tblz | UB#, LB# Enable to Low-Z output | 5 | | ns | 5 | | ns | 10 | | ns |
| | tolz | Output enable to Low-Z output | 5 | | ns | 5 | | ns | 5 | | ns |
| | thz | Chip enable to High-Z output | 0 | 20 | ns | 0 | 25 | ns | 0 | 20 | ns |
| | tbhz | UB#, LB# disable to High-Z output | 0 | 20 | ns | 0 | 25 | ns | 0 | 20 | ns |
| | tohz | Output disable to High-Z output | 0 | 20 | ns | 0 | 25 | ns | 0 | 20 | ns |
| | toh | Output hold from Address Change | 10 | | ns | 10 | | ns | 10 | | ns |
| | | | | | | | | | | | |

| | | | Asynchronous | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Version | B | | | | | | C | | |
| | | Performance Grade | -55 | | | -70 | | | -70 | | |
| | | Density | 8Mb pSRAM | | | 8Mb pSRAM | | | 8Mb pSRAM | | |
| 3 Volt | Symbol | Parameter | Min | Max | Units | Min | Max | Units | Min | Max | Units |
| Write | twc | Write cycle time | 55 | | ns | 70 | | ns | 70 | | ns |
| | tcw | Chip select to end of write | 45 | | ns | 55 | | ns | 70 | | ns |
| | tas | Address set up Time | 0 | | ns | 0 | | ns | 0 | | ns |
| | taw | Address valid to end of write | 45 | | ns | 55 | | ns | 70 | | ns |
| | tbw | UB#, LB# valid to end of write | 45 | | ns | 55 | | ns | 70 | | ns |
| | twp | Write pulse width | 45 | | ns | 55 | | ns | 55 | | ns |
| | twr | Write recovery time | 0 | | ns | 0 | | ns | 0 | | ns |
| | twhz | Write to output High-Z | | 25 | ns | | 25 | | | 20 | ns |
| | tdw | Data to write time overlap | 40 | | ns | 40 | | ns | 25 | | ns |
| | tdh | Data hold from write time | 0 | | ns | 0 | | ns | 0 | | ns |
| | tow | End write to output Low-Z | 5 | | | 5 | | | 5 | | |
| | tow | Write high pulse width | x | x | ns | x | x | ns | x | x | ns |
| | | | | | | | | | | | |
| Other | tpc | Page read cycle | x | | | x | | | x | | |
| | tpa | Page address access time | | x | | | x | | | x | |
| | twpc | Page write cycle | x | | | x | | | x | | |
| | tcp | Chip select high pulse width | x | | | x | | | x | | |

# AC Characteristics

## (16Mb pSRAM Asynchronous)

| | | | Asynchronous | | | | | |
|---|---|---|---|---|---|---|---|---|
| Performance Grade | | | -55 | | | -70 | | |
| Density | | | 16Mb pSRAM | | | 16Mb pSRAM | | |
| 3 Volt | Symbol | Parameter | Min | Max | Units | Min | Max | Units |
| Read | trc | Read cycle time | 55 | | ns | 70 | | ns |
| | taa | Address Access Time | | 55 | ns | | 70 | ns |
| | tco | Chip select to output | | 55 | ns | | 70 | ns |
| | toe | Output enable to valid output | | 30 | ns | | 35 | ns |
| | tba | UB#, LB# Access time | | 55 | ns | | 70 | ns |
| | tlz | Chip select to Low-z output | 5 | | ns | 5 | | ns |
| | tblz | UB#, LB# Enable to Low-Z output | 5 | | ns | 5 | | ns |
| | tolz | Output enable to Low-Z output | 5 | | ns | 5 | | ns |
| | thz | Chip enable to High-Z output | 0 | 25 | ns | 0 | 25 | ns |
| | tbhz | UB#, LB# disable to High-Z output | 0 | 25 | ns | 0 | 25 | ns |
| | tohz | Output disable to High-Z output | 0 | 25 | ns | 0 | 25 | ns |
| | toh | Output hold from Address Change | 10 | | ns | 10 | | ns |

| | | | Asynchronous | | | | | |
|---|---|---|---|---|---|---|---|---|
| Performance Grade | | | -55 | | | -70 | | |
| Density | | | 16Mb pSRAM | | | 16Mb pSRAM | | |
| 3 Volt | Symbol | Parameter | Min | Max | Units | Min | Max | Units |
| Write | twc | Write cycle time | 55 | | ns | 70 | | ns |
| | tcw | Chipselect to end of write | 50 | | ns | 55 | | ns |
| | tas | Address set up Time | 0 | | ns | 0 | | ns |
| | taw | Address valid to end of write | 50 | | ns | 55 | | ns |
| | tbw | UB#, LB# valid to end of write | 50 | | ns | 55 | | ns |
| | twp | Write pulse width | 50 | | ns | 55 | | ns |
| | twr | Write recovery time | 0 | | ns | 0 | | ns |
| | twhz | Write to output High-Z | | 25 | ns | | 25 | ns |
| | tdw | Data to write time overlap | 25 | | ns | 25 | | ns |
| | tdh | Data hold from write time | 0 | | ns | 0 | | ns |
| | tow | End write to output Low-Z | 5 | | | 5 | | |
| | tow | Write high pulse width | x | x | ns | x | x | ns |
| | | | | | | | | |
| Other | tpc | Page read cycle | x | | | x | | |
| | tpa | Page address access time | | x | | | x | |
| | twpc | Page write cycle | x | | | x | | |
| | tcp | Chip select high pulse width | x | | | x | | |

# AC Characteristics

## (16Mb pSRAM Page Mode)

| | | | Page Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Performance Grade | | | -60 | | | -65 | | | -70 | | |
| Density | | | 16Mb pSRAM | | | 16Mb pSRAM | | | 16Mb pSRAM | | |
| 3 Volt | Symbol | Parameter | Min | Max | Units | Min | Max | Units | Min | Max | Units |
| Read | trc | Read cycle time | 60 | 20k | ns | 65 | 20k | ns | 70 | 20k | ns |
| | taa | Address Access Time | | 60 | ns | | 65 | ns | | 70 | ns |
| | tco | Chip select to output | | 60 | ns | | 65 | ns | | 70 | ns |
| | toe | Output enable to valid output | | 25 | ns | | 25 | ns | | 25 | ns |
| | tba | UB#, LB# Access time | | 60 | ns | | 65 | ns | | 70 | ns |
| | tlz | Chip select to Low-z output | 10 | | ns | 10 | | ns | 10 | | ns |
| | tblz | UB#, LB# Enable to Low-Z output | 10 | | ns | 10 | | ns | 10 | | ns |
| | tolz | Output enable to Low-Z output | 5 | | ns | 5 | | ns | 5 | | ns |
| | thz | Chip enable to High-Z output | 0 | 5 | ns | 0 | 5 | ns | 0 | 5 | ns |
| | tbhz | UB#, LB# disable to High-Z output | 0 | 5 | ns | 0 | 5 | ns | 0 | 5 | ns |
| | tohz | Output disable to High-Z output | 0 | 5 | ns | 0 | 5 | ns | 0 | 5 | ns |
| | toh | Output hold from Address Change | 5 | | ns | 5 | | ns | 5 | | ns |

| | | | Page Mode | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Performance Grade | | | -60 | | | -65 | | | -70 | | |
| Density | | | 16Mb pSRAM | | | 16Mb pSRAM | | | 16Mb pSRAM | | |
| 3 Volt | Symbol | Parameter | Min | Max | Units | Min | Max | Units | Min | Max | Units |
| Write | twc | Write cycle time | 60 | 20k | ns | 65 | 20k | ns | 70 | 20k | ns |
| | tcw | Chipselect to end of write | 50 | | ns | 60 | | ns | 60 | | ns |
| | tas | Address set up Time | 0 | | ns | 0 | | ns | 0 | | ns |
| | taw | Address valid to end of write | 50 | | ns | 60 | | ns | 60 | | ns |
| | tbw | UB#, LB# valid to end of write | 50 | | ns | 60 | | ns | 60 | | ns |
| | twp | Write pulse width | 50 | | ns | 50 | | ns | 50 | | ns |
| | twr | Write recovery time | 0 | | ns | 0 | | ns | 0 | | ns |
| | twhz | Write to output High-Z | | 5 | ns | | 5 | ns | | 5 | ns |
| | tdw | Data to write time overlap | 20 | | ns | 20 | | ns | 20 | | ns |
| | tdh | Data hold from write time | 0 | | ns | 0 | | ns | 0 | | ns |
| | tow | End write to output Low-Z | 5 | | | 5 | | | 5 | | |
| | tow | Write high pulse width | 7.5 | | ns | 7.5 | | ns | 7.5 | | ns |
| | | | | | | | | | | | |
| Other | tpc | Page read cycle | 25 | 20k | ns | 25 | 20k | ns | 25 | 20k | ns |
| | tpa | Page address access time | | 25 | ns | | 25 | ns | | 25 | ns |
| | twpc | Page write cycle | 25 | 20k | ns | 25 | 20k | ns | 25 | 20k | ns |
| | tcp | Chip select high pulse width | 10 | | ns | 10 | | ns | 10 | | ns |

# AC Characteristics

## (32Mb pSRAM Page Mode)

| | | | Page Mode | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Version | C | | | E | | | | | | | | |
| | | Performance Grade | -65 | | | -60 | | | -65 | | | -70 | | |
| | | Density | 32Mb pSRAM | | | 32Mb pSRAM | | | 32Mb pSRAM | | | 32Mb pSRAM | | |
| 3 Volt | Symbol | Parameter | Min | Max | Units | Min | Max | Units | Min | Max | Units | Min | Max | Units |
| Read | trc | Read cycle time | 65 | 20k | ns | 60 | 20k | ns | 65 | 20k | ns | 70 | 20k | ns |
| | taa | Address Access Time | | 65 | ns | | 60 | ns | | 65 | ns | | 70 | ns |
| | tco | Chip select to output | | 65 | ns | | 60 | ns | | 65 | ns | | 70 | ns |
| | toe | Output enable to valid output | | 20 | ns | | 25 | ns | | 25 | ns | | 25 | ns |
| | tba | UB#, LB# Access time | | 65 | ns | | 60 | ns | | 65 | ns | | 70 | ns |
| | tlz | Chip select to Low-z output | 10 | | ns | 10 | | ns | 10 | | ns | 10 | | ns |
| | tblz | UB#, LB# Enable to Low-Z output | 10 | | ns | 10 | | ns | 10 | | ns | 10 | | ns |
| | tolz | Output enable to Low-Z output | 5 | | ns | 5 | | ns | 5 | | ns | 5 | | ns |
| | thz | Chip enable to High-Z output | 0 | 20 | ns | 0 | 5 | ns | 0 | 5 | ns | 0 | 5 | ns |
| | tbhz | UB#, LB# disable to High-Z output | 0 | 20 | ns | 0 | 5 | ns | 0 | 5 | ns | 0 | 5 | ns |
| | tohz | Output disable to High-Z output | 0 | 20 | ns | 0 | 5 | ns | 0 | 5 | ns | 0 | 5 | ns |
| | toh | Output hold from Address Change | 5 | | ns | 5 | | ns | 5 | | ns | 5 | | ns |

| | | | Page Mode | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Version | C | | | E | | | | | | | | |
| | | Performance Grade | -65 | | | -60 | | | -65 | | | -70 | | |
| | | Density | 32Mb pSRAM | | | 32Mb pSRAM | | | 32Mb pSRAM | | | 32Mb pSRAM | | |
| 3 Volt | Symbol | Parameter | Min | Max | Units | Min | Max | Units | Min | Max | Units | Min | Max | Units |
| Write | twc | Write cycle time | 65 | 20k | ns | 60 | 20k | ns | 65 | 20k | ns | 70 | 20k | ns |
| | tcw | Chipselect to end of write | 55 | | ns | 50 | | ns | 60 | | ns | 60 | | ns |
| | tas | Address set up Time | 0 | | ns | 0 | | ns | 0 | | ns | 0 | | ns |
| | taw | Address valid to end of write | 55 | | ns | 50 | | ns | 60 | | ns | 60 | | ns |
| | tbw | UB#, LB# valid to end of write | 55 | | ns | 50 | | ns | 60 | | ns | 60 | | ns |
| | twp | Write pulse width | 55 | 20k | ns | 50 | | ns | 50 | | ns | 50 | | ns |
| | twr | Write recovery time | 0 | | ns | 0 | | ns | 0 | | ns | 0 | | ns |
| | twhz | Write to output High-Z | | 5 | ns | | 5 | ns | | 5 | ns | | 5 | ns |
| | tdw | Data to write time overlap | 25 | | ns | 20 | | ns | 20 | | ns | 20 | | ns |
| | tdh | Data hold from write time | 0 | | ns | 0 | | ns | 0 | | ns | 0 | | ns |
| | tow | End write to output Low-Z | 5 | | | 5 | | | 5 | | | 5 | | |
| | tow | Write high pulse width | 7.5 | | ns | 7.5 | | ns | 7.5 | | ns | 7.5 | | ns |
| | | | | | | | | | | | | | | |
| Other | tpc | Page read cycle | 25 | 20k | ns | 25 | 20k | ns | 25 | 20k | ns | 25 | 20k | ns |
| | tpa | Page address access time | | 25 | ns | | 25 | ns | | 25 | ns | | 25 | ns |
| | twpc | Page write cycle | 25 | 20k | ns | 25 | 20k | ns | 25 | 20k | ns | 25 | 20k | ns |
| | tcp | Chip select high pulse width | 10 | | ns | 10 | | ns | 10 | | ns | 10 | | ns |

# AC Characteristics

## (64Mb pSRAM Page Mode)

| | | | Page Mode | | |
|---|---|---|---|---|---|
| | | Performance Grade | -70 | | |
| | | Density | 64Mb pSRAM | | |
| 3 Volt | Symbol | Parameter | Min | Max | Units |
| Read | trc | Read cycle time | 70 | 20k | ns |
| | taa | Address Access Time | | 70 | ns |
| | tco | Chip select to output | | 70 | ns |
| | toe | Output enable to valid output | | 25 | ns |
| | tba | UB#, LB# Access time | | 70 | ns |
| | tlz | Chip select to Low-z output | 10 | | ns |
| | tblz | UB#, LB# Enable to Low-Z output | 10 | | ns |
| | tolz | Output enable to Low-Z output | 5 | | ns |
| | thz | Chip enable to High-Z output | 0 | 5 | ns |
| | tbhz | UB#, LB# disable to High-Z output | 0 | 5 | ns |
| | tohz | Output disable to High-Z output | 0 | 5 | ns |
| | toh | Output hold from Address Change | 5 | | ns |

| | | | Page Mode | | |
|---|---|---|---|---|---|
| | | Performance Grade | -70 | | |
| | | Density | 64Mb pSRAM | | |
| 3 Volt | Symbol | Parameter | Min | Max | Units |
| Write | twc | Write cycle time | 70 | 20k | ns |
| | tcw | Chipselect to end of write | 60 | | ns |
| | tas | Address set up Time | 0 | | ns |
| | taw | Address valid to end of write | 60 | | ns |
| | tbw | UB#, LB# valid to end of write | 60 | | ns |
| | twp | Write pulse width | 50 | 20k | ns |
| | twr | Write recovery time | 0 | | ns |
| | twhz | Write to output High-Z | | 5 | ns |
| | tdw | Data to write time overlap | 20 | | ns |
| | tdh | Data hold from write time | 0 | | ns |
| | tow | End write to output Low-Z | 5 | | |
| | tow | Write high pulse width | 7.5 | | ns |
| | | | | | |
| Other | tpc | Page read cycle | 20 | 20k | ns |
| | tpa | Page address access time | | 20 | ns |
| | twpc | Page write cycle | 20 | 20k | ns |
| | tcp | Chip select high pulse width | 10 | | ns |

# Timing Diagrams

## Read Cycle

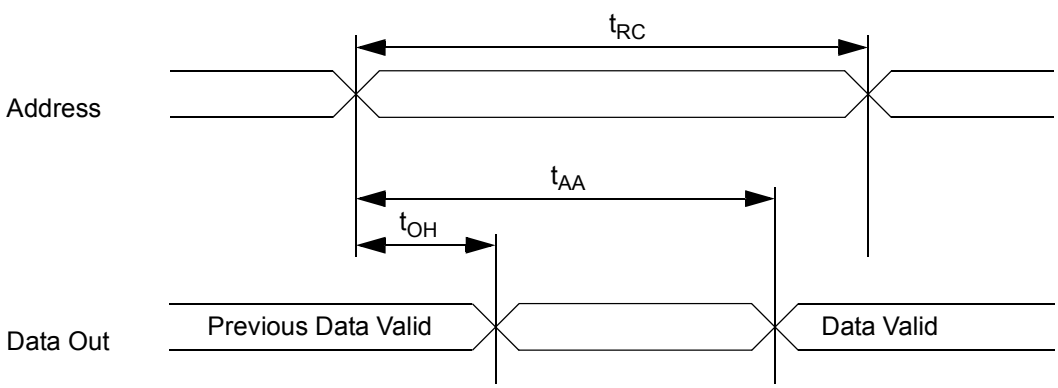



**Figure 22. Timing of Read Cycle (CE# = OE# = $V_{IL}$, WE# = ZZ# = $V_{IH}$)**

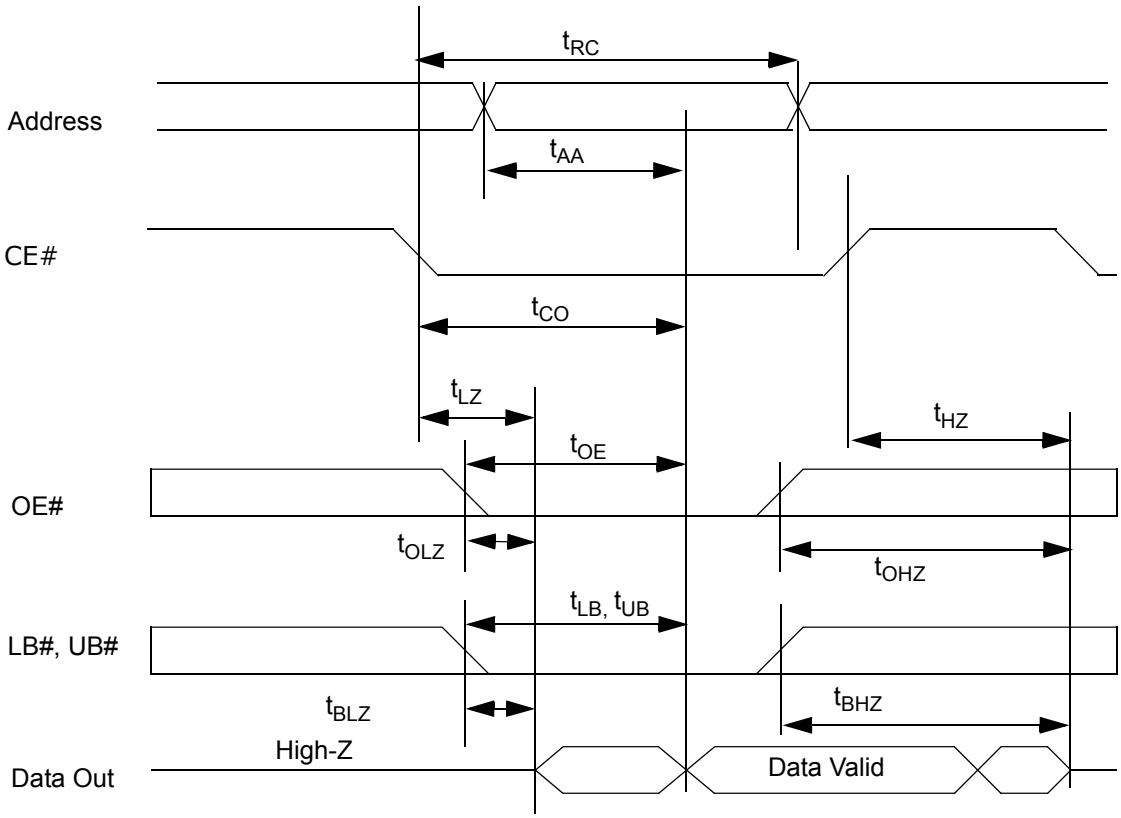



**Figure 23. Timing Waveform of Read Cycle (WE# = ZZ# = $V_{IH}$)**

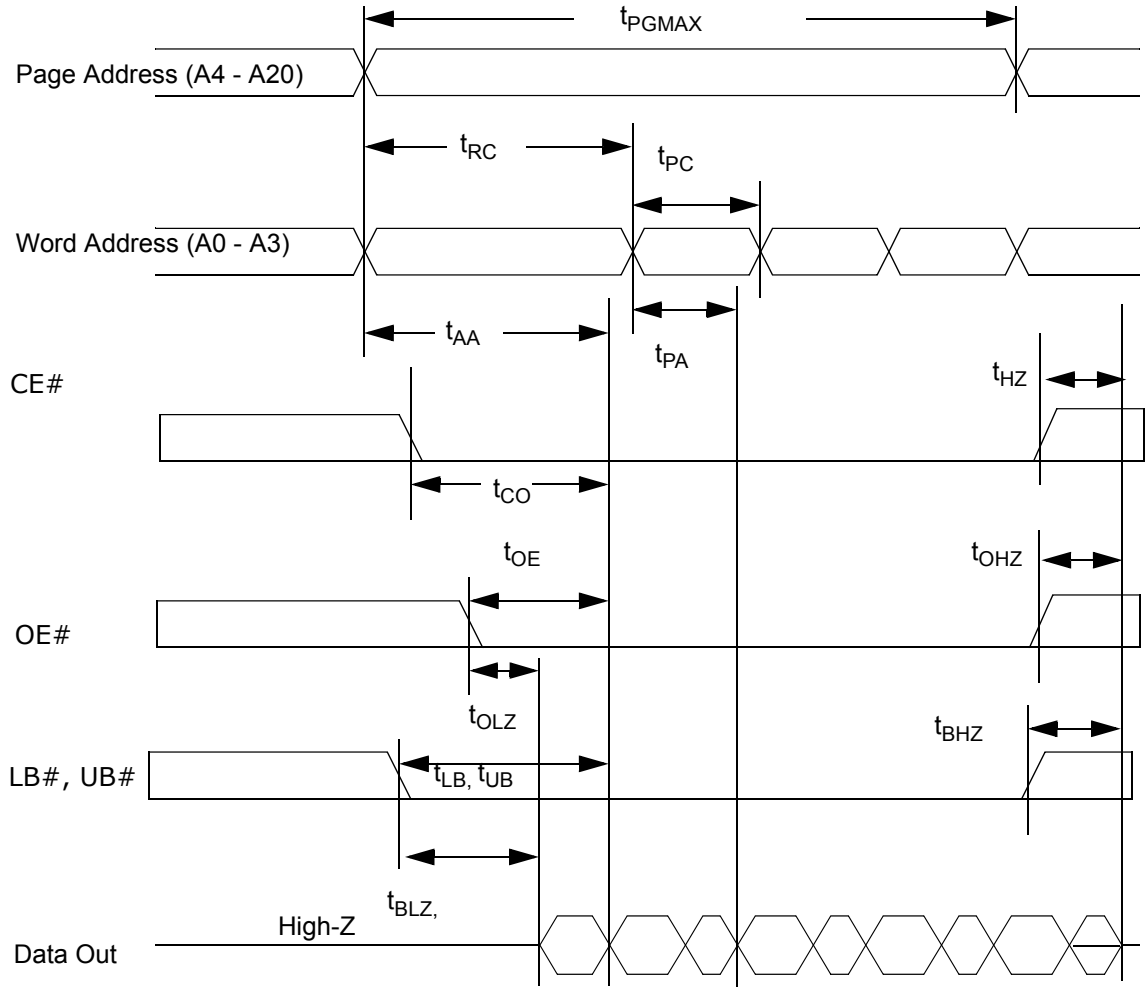



**Figure 24. Timing Waveform of Page Mode Read Cycle (WE# = ZZ# = $V_{IH}$)**

## Write Cycle

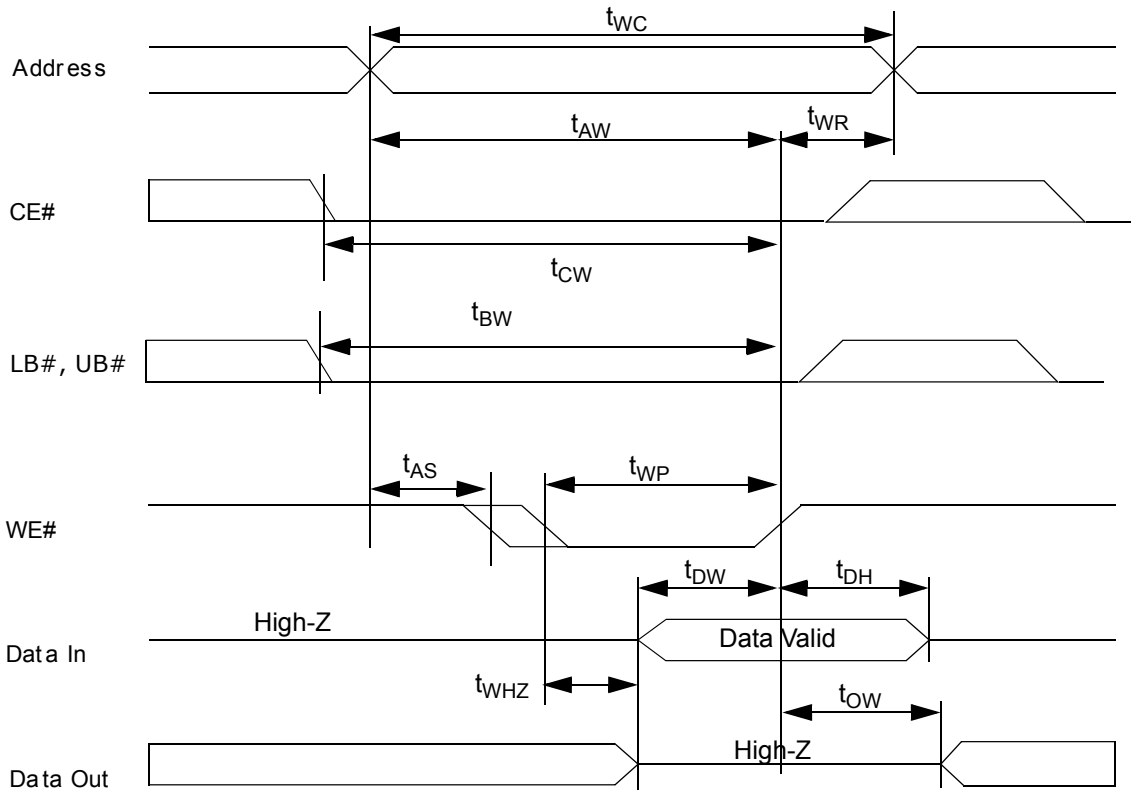



**Figure 25. Timing Waveform of Write Cycle (WE# Control, ZZ# = $V_{IH}$)**

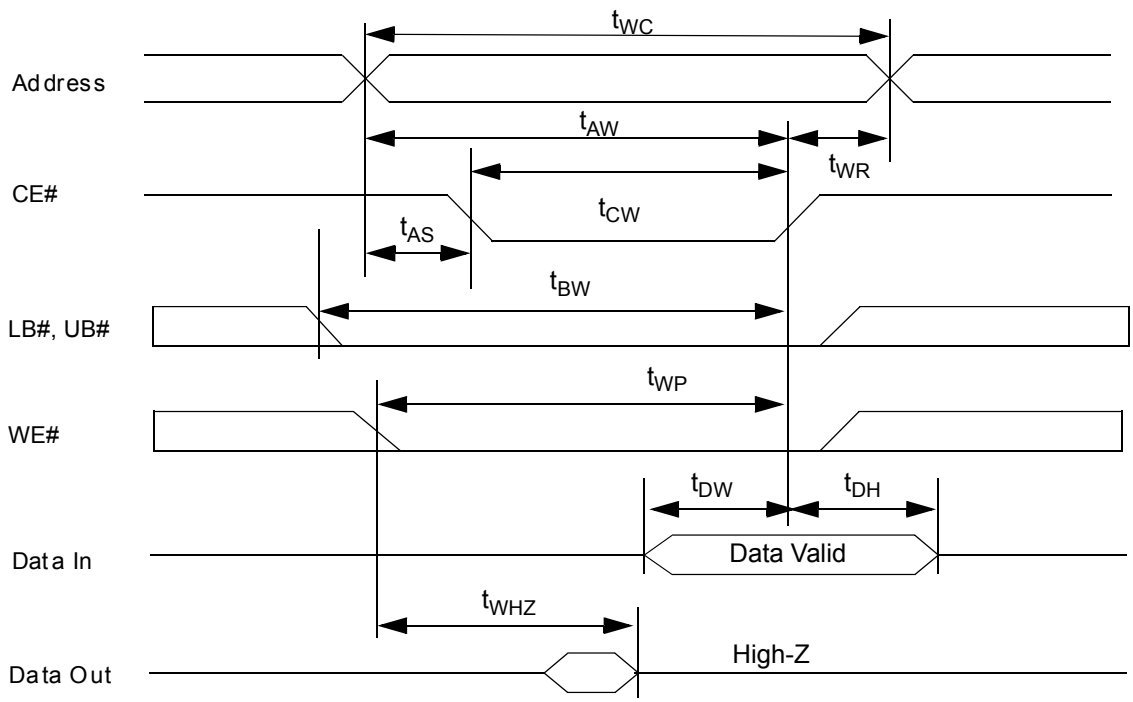



**Figure 26. Timing Waveform of Write Cycle (CE# Control, ZZ# = $V_{IH}$)**

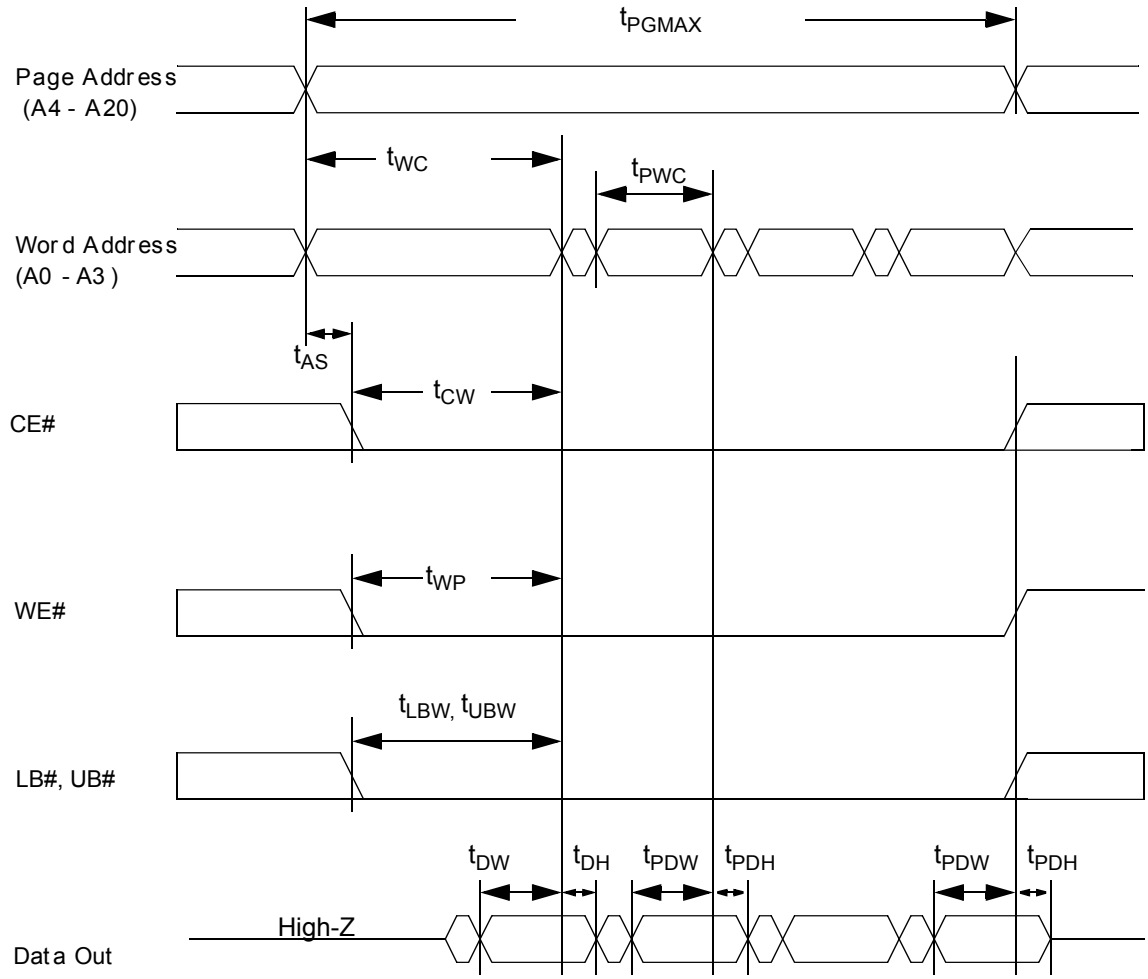



**Figure 27. Timing Waveform of Page Mode Write Cycle (ZZ# = $V_{IH}$)**

## Power Savings Modes (For 16M Page Mode, 32M and 64M Only)

There are several power savings modes.

- Partial Array Self Refresh
- Temperature Compensated Refresh (64M)
- Deep Sleep Mode
- Reduced Memory Size (32M, 16M)

The operation of the power saving modes ins controlled by the settings of bits contained in the Mode Register. This definition of the Mode Register is shown in Figure 28 and the various bits are used to enable and disable the various low power modes as well as enabling Page Mode operation. The Mode Register is set by using the timings defined in Figure xxx.

### Partial Array Self Refresh (PAR)

In this mode of operation, the internal refresh operation can be restricted to a 16Mb, 32Mb, or 48Mb portion of the array. The array partition to be refreshed is determined by the respective bit settings in the Mode Register. The register settings for the PASR operation are defined in Table xxx. In this PASR mode, when ZZ# is active low, only the portion of the array that is set in the register is re-

freshed. The data in the remainder of the array will be lost. The PASR operation mode is only available during standby time (ZZ# low) and once ZZ# is returned high, the device resumes full array refresh. All future PASR cycles will use the contents of the Mode Register that has been previously set. To change the address space of the PASR mode, the Mode Register must be reset using the previously defined procedures. For PASR to be activated, the register bit, A4 must be set to a one (1) value, "PASR Enabled". If this is the case, PASR will be activated 10 µs after ZZ# is brought low. If the A4 register bit is set equal to zero (0), PASR will not be activated.

## Temperature Compensated Refresh (for 64Mb)

In this mode of operation, the internal refresh rate can be optimized for the operation temperature used and this can then lower standby current. The DRAM array in the PSRAM must be refreshed internally on a regular basis. At higher temperatures, the DRAM cell must be refreshed more often than at lower temperatures. By setting the temperature of operation in the Mode Register, this refresh rate can be optimized to yield the lowest standby current at the given operating temperature. There are four different temperature settings that can be programmed in to the PSRAM. These are defined in Figure 28.

## Deep Sleep Mode

In this mode of operation, the internal refresh is turned off and all data integrity of the array is lost. Deep Sleep is entered by bringing ZZ# low with the A4 register bit set to a zero (0), "Deep Sleep Enabled". If this is the case, Deep Sleep will be entered 10 µs after ZZ# is brought low. The device will remain in this mode as long as ZZ# remains low. If the A4 register bit is set equal to one (1), Deep Sleep will not be activated.

## Reduced Memory Size (for 32M and 16M)

In this mode of operation, the 32Mb PSRAM can be operated as a 8Mb or 16Mb device. The mode and array size are determined by the settings in the VA register. The VA register is set according to the following timings and the bit settings in the table "Address Patterns for RMS". The RMS mode is enabled at the time of ZZ transitioning high and the mode remains active until the register is updated. To return to the full 32Mb address space, the VA register must be reset using the previously defined procedures. While operating in the RMS mode, the unselected portion of the array may not be used.

## Other Mode Register Settings (for 64M)

The Page Mode operation can also be enabled and disabled using the Mode Register. Register bit A7 controls the operation of Page Mode and setting this bit to a one (1), enables Page Mode. If the register bit A7 is set to a zero (0), Page Mode operation is disabled.

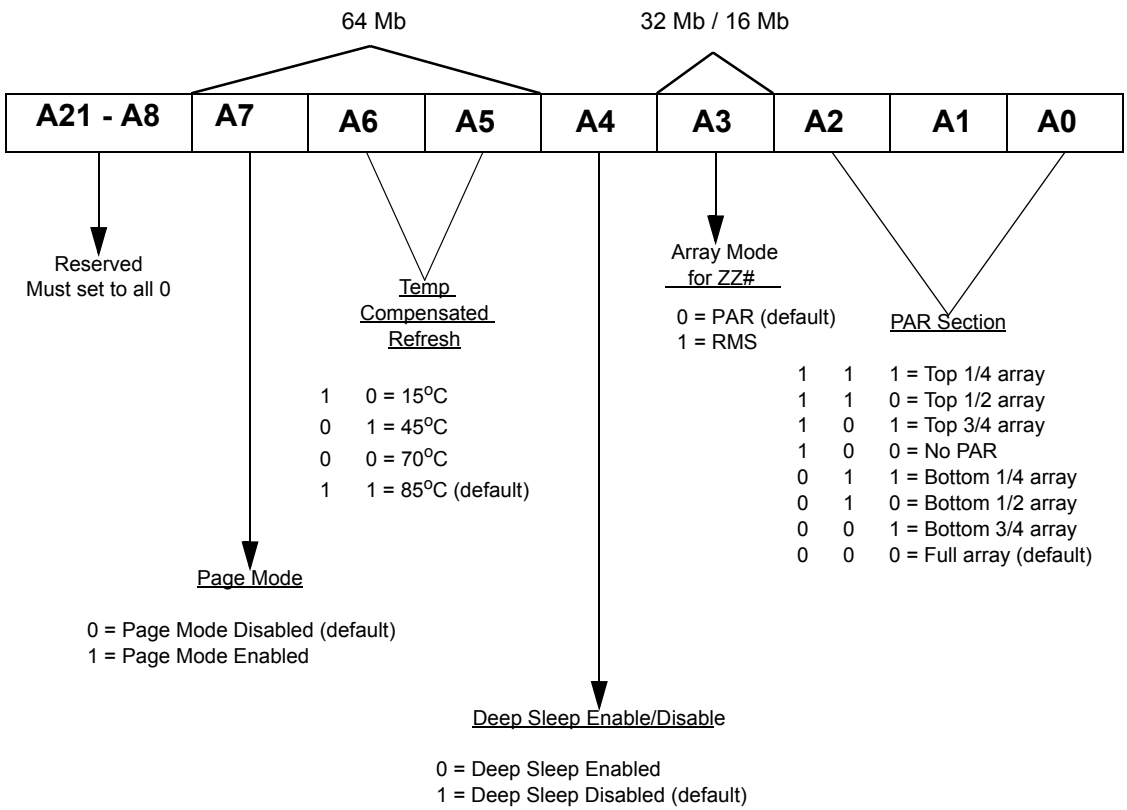



**Figure 28. Mode Register**

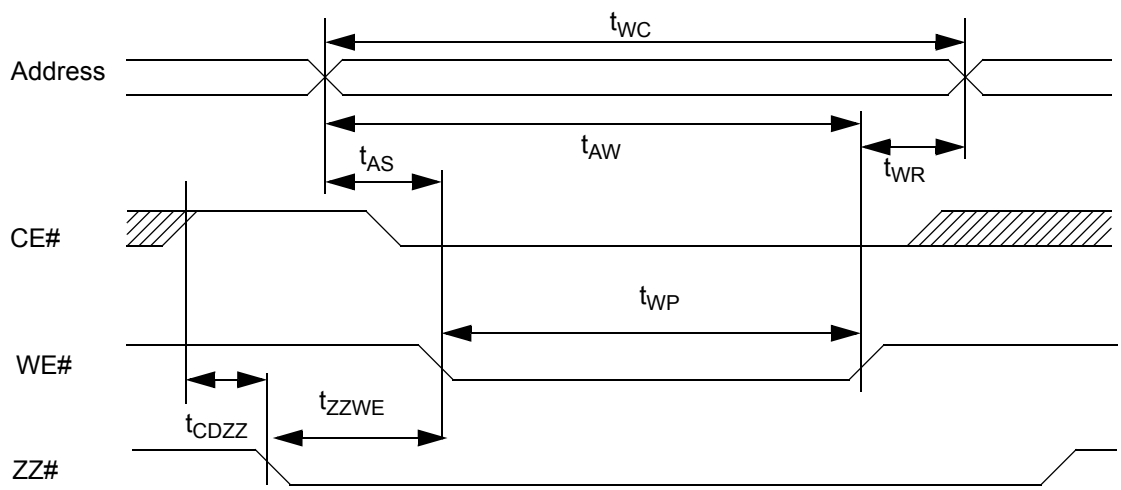



**Figure 29. Mode Register UpdateTimings (UB#, LB#, OE# are Don't Care)**

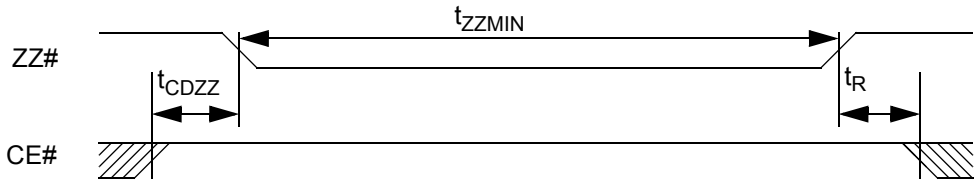



**Figure 30. Deep Sleep Mode - Entry/Exit Timings (for 64M)**

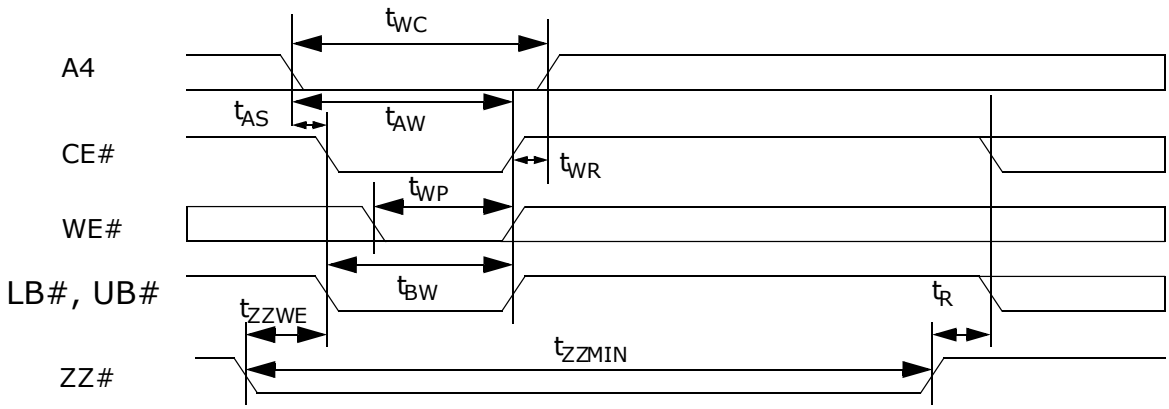



**Figure 31. Deep Sleep Mode - Entry/Exit Timings (for 32M and 16M)**

## Mode Register Update and Deep Sleep Timings

| Item | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Chip deselect to ZZ# low | $t_{CDZZ}$ | 5 | | ns | |
| ZZ# low to WE# low | $t_{ZZWE}$ | 10 | 500 | ns | |
| Write register cycle time | $t_{WC}$ | 70/85 | | ns | 1 |
| Chip enable to end of write | $t_{CW}$ | 70/85 | | ns | 1 |
| Address valid to end of write | $t_{AW}$ | 70/85 | | ns | 1 |
| Write recovery time | $t_{WR}$ | 0 | | ns | |
| Address setup time | $t_{AS}$ | 0 | | ns | |
| Write pulse width | $t_{WR}$ | 40 | | ns | |
| Deep Sleep Pulse Width | $t_{ZZMIN}$ | 10 | | µs | |
| Deep Sleep Recovery | $t_{R}$ | 200 | | µs | |

***Notes:***

*1. Minimum cycle time for writing register is equal to speed grade of product.*

## Address Patterns for PASR (A4=I) (64M)

| A2 | AI | A0 | Active Section | Address Space | Size | Density |
|---|---|---|---|---|---|---|
| 1 | 1 | 1 | Top quarter of die | 300000h-3FFFFFh | 1Mb x 16 | 16Mb |
| 1 | 1 | 0 | Top half of die | 200000h-3FFFFFh | 2Mb x 16 | 32Mb |
| 1 | 0 | 1 | Reserved | | | |
| 1 | 0 | 0 | No PASR | None | 0 | 0 |
| 0 | 1 | 1 | Bottom quarter of die | 000000h-0FFFFFh | 1Mb x 16 | 16Mb |
| 0 | 1 | 0 | Bottom half of die | 000000h-1FFFFFh | 2Mb x 16 | 32Mb |
| 0 | 0 | 1 | Reserved | | | |
| 0 | 0 | 0 | Full array | 000000h-3FFFFFh | 4Mb x 16 | 64Mb |

## Deep ICC Characteristics (for 64Mb)

| Item | Symbol | Test | Array Partition | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| PASR Mode Standby Current | $I_{PASR}$ | $V_{IN}$ = $V_{CC}$ or 0V, Chip Disabled, $t_A$ = 85°C | None | | 10 | µA |
| | | | 1/4 Array | | 60 | |
| | | | 1/2 Array | | 80 | |
| | | | Full Array | | 120 | |

| Item | Symbol | Max Temperature | Typ | Max | Unit |
|---|---|---|---|---|---|
| Temperature Compensated Refresh Current | $I_{TCR}$ | 15°C | | 50 | µA |
| | | 45°C | | 60 | |
| | | 70°C | | 80 | |
| | | 85°C | | 120 | |

| Item | Symbol | Test | Typ | Max | Unit |
|---|---|---|---|---|---|
| Deep Sleep Current | $I_{ZZ}$ | $V_{IN}$ = $V_{CC}$ or 0V, Chip in ZZ# mode, $t_A$ = 25°C | | 10 | µA |

## Address Patterns for PAR (A3= 0, A4=I) (32M)

| A2 | AI | A0 | Active Section | Address Space | Size | Density |
|---|---|---|---|---|---|---|
| 0 | 1 | 1 | One-quarter of die | 000000h - 07FFFFh | 512Kb x 16 | 8Mb |
| 0 | 1 | 0 | One-half of die | 000000h - 0FFFFFh | 1Mb x 16 | 16Mb |
| x | 0 | 0 | Full die | 000000h - 1FFFFFh | 2Mb x 16 | 32Mb |
| 1 | 1 | 1 | One-quarter of die | 180000h - 1FFFFFh | 512Kb x 16 | 8Mb |
| 1 | 1 | 0 | One-half of die | 100000h - 1FFFFFh | 1Mb x 16 | 16Mb |

## Address Patterns for RMS (A3 = I, A4 = I) (32M)

| A2 | AI | A0 | Active Section | Address Space | Size | Density |
|---|---|---|---|---|---|---|
| 0 | 1 | 1 | One-quarter of die | 000000h - 07FFFFh | 512Kb x 16 | 8Mb |
| 0 | 1 | 0 | One-half of die | 000000h - 0FFFFFh | 1Mb x 16 | 16Mb |
| 1 | 1 | 1 | One-quarter of die | 180000h - 1FFFFFh | 512Kb x 16 | 8Mb |
| 1 | 1 | 0 | One-half of die | 100000h - 1FFFFFh | 1Mb x 16 | 16Mb |

## Low Power ICC Characteristics (32M)

| Item | Symbol | Test | Array Partition | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| PAR Mode Standby Current | $I_{PAR}$ | $V_{IN}$ = $V_{CC}$ or 0V, Chip Disabled, $t_A$= 85°C | 1/4 Array | | 75 | µA |
| | | | 1/2 Array | | 90 | µA |
| RMS Mode Standby Current | $I_{RMSSB}$ | $V_{IN}$ = $V_{CC}$ or 0V, Chip Disabled, $t_A$= 85°C | 8Mb Device | | 75 | µA |
| | | | 16Mb Device | | 90 | µA |
| Deep Sleep Current | $I_{ZZ}$ | $V_{IN}$ = $V_{CC}$ or 0V, Chip in $\overline{ZZ}$ mode, $t_A$= 85°C | | | 10 | µA |

## Address Patterns for PAR (A3= 0, A4=I) (16M)

| A2 | AI | A0 | Active Section | Address Space | Size | Density |
|---|---|---|---|---|---|---|
| 0 | 1 | 1 | One-quarter of die | 00000h - 0FFFFh | 256Kb x 16 | 4Mb |
| 0 | 1 | 0 | One-half of die | 00000h - 7FFFFh | 512Kb x 16 | 8Mb |
| x | 0 | 0 | Full die | 00000h - FFFFFh | 1Mb x 16 | 16Mb |
| 1 | 1 | 1 | One-quarter of die | C0000h - FFFFh | 256Kb x 16 | 4Mb |
| 1 | 1 | 0 | One-half of die | 80000h - 1FFFFFh | 512Kb x 16 | 8Mb |

## Address Patterns for RMS (A3 = I, A4 = I) (16M)

| A2 | AI | A0 | Active Section | Address Space | Size | Density |
|---|---|---|---|---|---|---|
| 0 | 1 | 1 | One-quarter of die | 00000h - 0FFFFh | 256Kb x 16 | 4Mb |
| 0 | 1 | 0 | One-half of die | 00000h - 7FFFFh | 512Kb x 16 | 8Mb |
| 1 | 1 | 1 | One-quarter of die | C0000h - FFFFFh | 256Kb x 16 | 4Mb |
| 1 | 1 | 0 | One-half of die | 80000h - FFFFFh | 512Kb x 16 | 8Mb |

## Low Power ICC Characteristics (16M)

| Item | Symbol | Test | Array Partition | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| PAR Mode Standby Current | $I_{PAR}$ | $V_{IN}$ = $V_{CC}$ or 0V, Chip Disabled, $t_A$= 85°C | 1/4 Array | | 65 | µA |
| | | | 1/2 Array | | 80 | |
| RMS Mode Standby Current | $I_{RMSSB}$ | $V_{IN}$ = $V_{CC}$ or 0V, Chip Disabled, $t_A$= 85°C | 4Mb Device | | 65 | µA |
| | | | 8Mb Device | | 80 | |
| Deep Sleep Current | $I_{ZZ}$ | $V_{IN}$ = $V_{CC}$ or 0V, Chip in ZZ# mode, $t_A$= 85°C | | | 10 | µA |

# pSRAM Type 7

## 16Mb (1M word x 16-bit)

## 32Mb (2M word x 16-bit)

## 64Mb (4M word x 16-bit)

## CMOS 1M/2M/4M-Word x 16 bit Fast Cycle Random Access Memory with Low Power SRAM Interface

## Features

- Asynchronous SRAM Interface
- Fast Access Time
  - tCE = tAA = 60ns max (16M)
  - tCE = tAA = 65ns max (32M/64M)
- 8 words Page Access Capability
  - tPAA = 20ns max (32M/64M)
- Low Voltage Operating Condition
  - VDD = +2.7V to +3.1V
- Wide Operating Temperature
  - TA = -30°C to +85°C
- Byte Control by LB and UB
- Low Power Consumption
  - IDDA1 = 20mA max (16M)
  - IDDA1 = 30mA max (32M)
  - IDDA1 =TBDmA max (64M)
  - IDDS1 = 100µA max (16M)
  - IDDS1 = 80µA max (32M)
  - IDDS1 = TBDµA max (64M)
- Various Power Down mode
  - Sleep, 4M-bit Partial or 8M-bit Partial (32M)
  - Sleep, 8M-bit Partial or 16M-bit Partial (64M

## Pin Description

| Pin Name | Description |
|---|---|
| $A_{21}$ to $A_0$ | Address Input : $A_{19}$ to $A_0$ for 16M, $A_{20}$ to $A_0$ for 32M, $A_{21}$ to $A_0$ for 64M |
| CE1# | Chip Enable (Low Active) |
| CE2# | Chip Enable (High Active) |
| WE# | Write Enable (Low Active) |
| OE# | Output Enable (Low Active) |
| UB# | Upper Byte Control (Low Active) |
| LB# | Lower Byte Control (Low Active) |
| $DQ_{16-9}$ | Upper Byte Data Input/Output |
| $DQ_{8-1}$ | Lower Byte Data Input/Output |
| $V_{DD}$ | Power Supply |

| Pin Name | Description |
|---|---|
| $V_{SS}$ | Ground |

# Functional Description

| Mode | CE2# | CE1# | WE# | OE# | LB# | UB# | $A_{21-0}$ | $DQ_{8-1}$ | $DQ_{16-9}$ |
|---|---|---|---|---|---|---|---|---|---|
| Standby (Deselect) | H | H | X | X | X | X | X | High-Z | High-Z |
| Output Disable (Note 1) | H | L | H | H | X | X | Note 3 | High-Z | High-Z |
| Output Disable (No Read) | | | H | L | H | H | Valid | High-Z | High-Z |
| Read (Upper Byte) | | | | | H | L | Valid | High-Z | Output Valid |
| Read (Lower Byte) | | | | | L | H | Valid | Output Valid | High-Z |
| Read (Word) | | | | | L | L | Valid | Output Valid | Output Valid |
| No Write | | | L | H (Note 4) | H | H | Valid | Invalid | Invalid |
| Write (Upper Byte) | | | | | H | L | Valid | Invalid | Input Valid |
| Write (Lower Byte) | | | | | L | H | Valid | Input Valid | Invalid |
| Write (Word) | | | | | L | L | Valid | Input Valid | Input Valid |
| Power Down | L | X | X | X | X | X | X | High-Z | High-Z |

***Legend:****L = $V_{IL}$, H = $V_{IH}$, X can be either $V_{IL}$ or $V_{IH}$, High-Z = High Impedence.*

***Notes:***

1. *Should not be kept this logic condition longer than 1ms. Please contact local Spansion representative for the relaxation of 1ms limitation.*
2. *Power Down mode can be entered from Standby state and all DQ pins are in High-Z state. Data retention depends on the selection of Power Down Program, 16M has data retetion in all modes except Power Down. Refer to POWER DOWN for the detail.*
3. *Can be either $V_{IL}$ or $V_{IH}$ but must be valid before Read or Write.*
4. *OE# can be $V_{IL}$ during Write operation if the following conditions are satisfied:*
   *(1) Write pulse is initiated by CE1# (refer to CE1# Controlled Write timing), or cycle time of the previous operation cycle is satisfied.*
   *(2) OE# stays $V_{IL}$ during Write cycle*

# Power Down (for 32M, 64M Only)

## Power Down

The Power Down is low power idle state controlled by CE2. CE2 Low drives the device in power down mode and maintains low power idle state as long as CE2 is kept Low. CE2 High resumes the device from power down mode. These devices have three power down mode. These can be proammed by series of read/write operation. Each mode has follwoing features.

| 32M | | | 64M | | |
|---|---|---|---|---|---|
| Mode | Retention Data | Retention Address | Mode | Retention Data | Retention Address |
| Sleep (default) | No | N/A | Sleep (default) | No | N/A |
| 4M Partial | 4M bit | 00000h to 3FFFFh | 8M Partial | 8M bit | 00000h to 7FFFFh |
| 8M Partial | 8M bit | 00000h to 7FFFFh | 16M Partial | 16M bit | 00000h to FFFFFh |

The default state is Sleep and it is the lowest power consumption but all data will be lost once CE2 is brought to Low for Power Down. It is not required to program to Sleep mode after power-up.

## Power Down Program Sequence

The program requires total 6 read/write operation with unique address. Between each read/write operation requires that device be in standby mode. Following table shows the detail sequence.

| Cycle # | Operation | Address | Data |
|---|---|---|---|
| 1st | Read | 3FFFFFh (MSB) | Read Data (RDa) |
| 2nd | Write | 3FFFFFh | RDa |
| 3rd | Write | 3FFFFFh | RDa |
| 4th | Write | 3FFFFFh | Don't Care (X) |
| 5th | Write | 3FFFFFh | X |
| 6th | Read | Address Key | Read Data (RDb) |

The first cycle is to read from most significient address (MSB).

The second and third cycle are to write back the data (RDa) read by first cycle. If the second or third cycle is written into the different address, the program is cancelled and the data written by the second or third cycle is valid as a normal write operation.

The forth and fifth cycle is to write to MSB. The data of forth and fifth cycle is don't-care. If the forth or fifth cycle is written into different address, the program is also cancelled but write data may not be wrote as normal write operation.

The last cycle is to read from specific address key for mode selection.

Once this program sequence is performed from a Partial mode to the other Partial mode, the written data stored in memory cell array may be lost. So, it should perform this program prior to regular read/write operation if Partial mode is used.

## Address Key

The address key has following format.

| Mode | | Address | | | | |
|---|---|---|---|---|---|---|
| 32M | 64M | A21 | A20 | A19 | A18 - A0 | Binary |
| Sleep (default) | Sleep (default) | 1 | 1 | 1 | 1 | 3FFFFFh |
| 4M Partial | N/A | 1 | 1 | 0 | 1 | 37FFFFh |
| 8M Partial | 8M Partial | 1 | 0 | 1 | 1 | 2FFFFFh |
| N/A | 16M Partial | 1 | 0 | 0 | 1 | 27FFFFh |

## Absolute Maximum Ratings

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Voltage of $V_{DD}$ Supply Relative to $V_{SS}$ | $V_{DD}$ | -0.5 to +3.6 | V |
| Voltage at Any Pin Relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | -0.5 to +3.6 | V |
| Short Circuit Output Current | $I_{OUT}$ | ±50 | mA |
| Storage temperature | $T_{STG}$ | -55 to +125 | °C |

*WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.*

## Recommended Operating Conditions (See Warning Below)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 2.7 | 3.1 | V |
| | $V_{SS}$ | 0 | 0 | V |
| High Level Input Voltage (Note 1) | $V_{IH}$ | $V_{DD}$ 0.8 | $V_{DD}$+0.2 | V |
| High Level Input Voltage (Note 1) | $V_{IL}$ | -0.3 | $V_{DD}$ 0.2 | V |
| Ambient Temperature | $T_A$ | -30 | 85 | °C |

***Notes:***

1. *Maximum DC voltage on input and I/O pins are $V_{DD}$+0.2V. During voltage transitions, inputs may positive overshoot to $V_{DD}$+1.0V for periods of up to 5 ns.*
2. *Minimum DC voltage on input or I/O pins are -0.3V. During voltage transitions, inputs may negative overshoot $V_{SS}$ to -1.0V for periods of up to 5ns.*

*WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.*

*Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.*

*No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.*

## Package Capacitance

Test conditions: $T_A$ = 25°C, f = 1.0 MHz

| Symbol | Description | Test Setup | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN1}$ | Address Input Capacitance | $V_{IN}$ = 0V | — | 5 | pF |
| $C_{IN2}$ | Control Input Capacitance | $V_{IN}$ = 0V | — | 5 | pF |
| $C_{IO}$ | Data Input/Output Capacitance | $V_{IO}$ = 0V | — | 8 | pF |

## DC Characteristics (Under Recommended Conditions Unless Otherwise Noted)

| Parameter | Symbol | Test Conditions | | 16M | | 32M | | 64M | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Input Leakage Current | $I_{LI}$ | $V_{IN}$ = $V_{SS}$ to $V_{DD}$ | | -1.0 | +1.0 | -1.0 | +1.0 | -1.0 | +1.0 | µA |
| Output Leakage Current | $I_{LO}$ | $V_{OUT}$ = $V_{SS}$ to $V_{DD}$, Output Disable | | -1.0 | +1.0 | -1.0 | +1.0 | -1.0 | +1.0 | µA |
| Output High Voltage Level | $V_{OH}$ | $V_{DD}$ = $V_{DD}$(min), $I_{OH}$ = –0.5mA | | 2.2 | — | 2.4 | — | 2.4 | — | V |
| Output Low Voltage Level | $V_{OL}$ | $I_{OL}$ = 1mA | | — | 0.4 | — | 0.4 | — | 0.4 | V |
| $V_{DD}$ Power Down Current | $I_{DDPS}$ | $V_{DD}$ = $V_{DD(26)}$ max., $V_{IN}$ = $V_{IH}$ or $V_{IL}$, CE2 ≤ 0.2V | SLEEP | | 10 | — | 10 | — | TBD | µA |
| | $I_{DDP4}$ | | 4M Partial | N/A | | — | 40 | N/A | | µA |
| | $I_{DDP8}$ | | 8M Partial | N/A | | — | 50 | — | TBD | µA |
| | $I_{DDP16}$ | | 16M Partial | N/A | | N/A | | — | TBD | µA |
| $V_{DD}$ Standby Current | $I_{DDS}$ | $V_{DD}$ = $V_{DD(26)}$ max., $\overline{V_{IN}}$ = $V_{IH}$ or $V_{IL}$, $\overline{CE1}$ = CE2 = $V_{IH}$ | | — | 1 | — | 1.5 | — | TBD | mA |
| | $I_{DDS1}$ | $V_{DD}$ = $V_{DD(26)}$ max., $\overline{V_{IN}}$ ≤ 0.2V or $V_{IN}$ ≥ $V_{DD}$ – 0.2V, $\overline{CE1}$ = CE2 ≥ $V_{DD}$ – 0.2V | | — | 100 | — | 80 | — | TBD | µA |
| $V_{DD}$ Active Current | $I_{DDA1}$ | $V_{DD}$ = $V_{DD(26)}$ max., $\overline{V_{IN}}$ = $V_{IH}$ or $V_{IL}$, $\overline{CE1}$ = $V_{IL}$ and CE2= $V_{IH}$, $I_{OUT}$=0mA | $t_{RC}$ / $t_{WC}$ = minimum | — | 20 | — | 30 | — | TBD | mA |
| | $I_{DDA2}$ | | $t_{RC}$ / $t_{WC}$ = 1µs | — | 3 | — | 3 | — | TBD | mA |
| $V_{DD}$ Page Read Current | $I_{DDA3}$ | $V_{DD}$ = $V_{DD(26)}$ max., $V_{IN}$ = $V_{IH}$ or $V_{IL}$, $\overline{CE1}$ = $V_{IL}$ and CE2= $V_{IH}$, $I_{OUT}$=0mA, $t_{PRC}$ = min. | | N/A | | — | 10 | — | TBD | mA |

***Notes:***

1. *All voltages are referenced to $V_{SS}$.*
2. *DC Characteristics are measured after following POWER-UP timing.*
3. *$I_{OUT}$ depends on the output load conditions.*

# AC Characteristics (Under Recommended Operating Conditions Unless Otherwise Noted)

## Read Operation

| Parameter | Symbol | 16M | | 32M | | 64M | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | | |
| Read Cycle Time | $t_{RC}$ | 70 | 1000 | 65 | 1000 | 65 | 1000 | ns | 1, 2 |
| CE1# Access Time | $t_{CE}$ | — | 60 | — | 65 | — | 65 | ns | 3 |
| OE# Access Time | $t_{OE}$ | — | 40 | — | 40 | — | 40 | ns | 3 |
| Address Access Time | $t_{AA}$ | — | 60 | — | 65 | — | 65 | ns | 3, 5 |
| LB# / UB# Access Time | $t_{BA}$ | — | 30 | — | 30 | — | 30 | ns | 3 |
| Page Address Access Time | $t_{PAA}$ | N/A | | — | 20 | — | 20 | ns | 3,6 |
| Page Read Cycle Time | $t_{PRC}$ | N/A | | 20 | 1000 | 20 | 1000 | ns | 1, 6, 7 |
| Output Data Hold Time | $t_{OH}$ | 5 | — | 5 | — | 5 | — | ns | 3 |
| CE1# Low to Output Low-Z | $t_{CLZ}$ | 5 | — | 5 | — | 5 | — | ns | 4 |
| OE# Low to Output Low-Z | $t_{OLZ}$ | 0 | — | 0 | — | 0 | — | ns | 4 |
| LB# / UB# Low to Output Low-Z | $t_{BLZ}$ | 0 | — | 0 | — | 0 | — | ns | 4 |
| CE1# High to Output High-Z | $t_{CHZ}$ | — | 20 | — | 20 | — | 20 | ns | 3 |
| OE# High to Output High-Z | $t_{OHZ}$ | — | 20 | — | 15 | — | 20 | ns | 3 |
| LB# / UB# High to Output High-Z | $t_{BHZ}$ | — | 20 | — | 20 | — | 20 | ns | 3 |
| Address Setup Time to CE1# Low | $t_{ASC}$ | -5 | — | –5 | — | –5 | — | ns | |
| Address Setup Time to OE# Low | $t_{ASO}$ | 10 | — | 10 | — | 10 | — | ns | |
| Address Invalid Time | $t_{AX}$ | — | 10 | — | 10 | — | 10 | ns | 5, 8 |
| Address Hold Time from CE1# High | $t_{CHAH}$ | -6 | — | –6 | — | –6 | — | ns | 9 |
| Address Hold Time from OE# High | $t_{OHAH}$ | -6 | — | –6 | — | –6 | — | ns | |
| WE# High to OE# Low Time for Read | $t_{WHOL}$ | 10 | 1000 | 12 | — | 12 | — | ns | 10 |
| CE1# High Pulse Width | $t_{CP}$ | 10 | — | 12 | — | 12 | — | ns | |

***Notes:***

1. *Maximum value is applicable if CE#1 is kept at Low without change of address input of A3 to A21. If needed by system operation, please contact local Spansion representative for the relaxation of 1µs limitation.*
2. *Address should not be changed within minimum $t_{RC}$.*
3. *The output load 50pF.*
4. *The output load 5pF.*

5. *Applicable to A3 to A21 (32M and 64M) when CE1# is kept at Low.*
6. *Applicable only to A0, A1 and A2 (32M and 64M) when CE1# is kept at Low for the page address access.*
7. *In case Page Read Cycle is continued with keeping CE1# stays Low, CE1# must be brought to High within 4µs. In other words, Page Read Cycle must be closed within 4µs.*
8. *Applicable when at least two of address inputs among applicable are switched from previous state.*
9. *$t_{RC}$(min) and $t_{PRC}$(min) must be satisfied.*
10. *If actual value of $t_{WHOL}$ is shorter than specified minimum values, the actual $t_{AA}$ of following Read may become longer by the amount of subtracting actual value from specified minimum value.*

# AC Characteristics

## Write Operation

| Parameter | Symbol | 16M | | 32M | | 64M | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Write Cycle Time | $t_{WC}$ | 70 | 1000 | 65 | 1000 | 65 | 1000 | ns | 1,2 |
| Address Setup Time | $t_{AS}$ | 0 | — | 0 | — | 0 | — | ns | 3 |
| CE1# Write Pulse Width | $t_{CW}$ | 45 | — | 40 | — | 40 | — | ns | 3 |
| WE# Write Pulse Width | $t_{WP}$ | 45 | — | 40 | — | 40 | — | ns | 3 |
| LB#/UB# Write Pulse Width | $t_{BW}$ | 45 | — | 40 | — | 40 | — | ns | 3 |
| LB#/UB# Byte Mask Setup Time | $t_{BS}$ | -5 | — | –5 | — | –5 | — | ns | 4 |
| LB#/UB# Byte Mask Hold Time | $t_{BH}$ | -5 | — | –5 | — | –5 | — | ns | 5 |
| Write Recovery Time | $t_{WR}$ | 0 | — | 0 | — | 0 | — | ns | 6 |
| CE1# High Pulse Width | $t_{CP}$ | 10 | — | 12 | — | 12 | — | ns | |
| WE# High Pulse Width | $t_{WHP}$ | 7.5 | 1000 | 7.5 | 1000 | 7.5 | 1000 | ns | 7 |
| LB#/UB# High Pulse Width | $t_{BHP}$ | 10 | 1000 | 12 | 1000 | 12 | 1000 | ns | |
| Data Setup Time | $t_{DS}$ | 15 | — | 12 | — | 12 | — | ns | |
| Data Hold Time | $t_{DH}$ | 0 | — | 0 | — | 0 | — | ns | |
| OE# High to CE1# Low Setup Time for Write | $t_{OHCL}$ | -5 | — | –5 | — | –5 | — | ns | 8 |
| OE# High to Address Setup Time for Write | $t_{OES}$ | 0 | — | 0 | — | 0 | — | ns | 9 |
| LB# and UB# Write Pulse Overlap | $t_{BWO}$ | 30 | — | 30 | — | 30 | — | ns | |

***Notes:***

1. *Maximum value is applicable if CE1# is kept at Low without any address change. If the relaxation is needed by system operation, please contact local Spansion representative for the relaxation of 1µs limitation.*
2. *Minimum value must be equal or greater than the sum of write pulse ($t_{CW}$, $t_{WP}$ or $t_{BW}$) and write recovery time ($t_{WR}$).*
3. *Write pulse is defined from High to Low transition of CE1#, WE#, or LB#/UB#, whichever occurs last.*
4. *Applicable for byte mask only. Byte mask setup time is defined to the High to Low transition of CE1# or WE# whichever occurs last.*
5. *Applicable for byte mask only. Byte mask hold time is defined from the Low to High transition of CE1# or WE# whichever occurs first.*
6. *Write recovery is defined from Low to High transition of CE1#, WE#, or LB#/UB#, whichever occurs first.*
7. *$t_{WPH}$ minimum is absolute minimum value for device to detect High level. And it is defined at minimum $V_{IH}$ level.*
8. *If OE# is Low after minimum $t_{OHCL}$, read cycle is initiated. In other words, OE# must be brought to High within 5ns after CE1# is brought to Low. Once read cycle is initiated, new write pulse should be input after minimum $t_{RC}$ is met.*
9. *If OE# is Low after new address input, read cycle is initiated. In other word, OE# must be brought to High at the same time or before new address valid. Once read cycle is initiated, new write pulse should be input after minimum $t_{RC}$ is met and data bus is in High-Z.*

# AC Characteristics

## Power Down Parameters

| Parameter | Symbol | 16M | | 32M | | 64M | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| CE2 Low Setup Time for Power Down Entry | $t_{CSP}$ | 10 | — | 10 | — | 10 | — | ns | |
| CE2 Low Hold Time after Power Down Entry | $t_{C2LP}$ | 80 | — | 65 | — | 65 | — | ns | |
| CE1# High Hold Time following CE2 High after Power Down Exit [SLEEP mode only] | $t_{CHH}$ | 300 | — | 300 | — | 300 | — | µs | 1 |
| CE1# High Hold Time following CE2 High after Power Down Exit [not in SLEEP mode] | $t_{CHHP}$ | N/A | | 1 | — | 1 | — | µs | 2 |
| CE1# High Setup Time following CE2 High after Power Down Exit | $t_{CHS}$ | 0 | — | 0 | — | 0 | — | ns | 1 |

***Notes:***

1. *Applicable also to power-up.*
2. *Applicable when 4M and 8M Partial mode is programmed.*

## Other Timing Parameters

| Parameter | Symbol | 16M | | 32M | | 64M | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| CE1# High to OE# Invalid Time for Standby Entry | $t_{CHOX}$ | 10 | — | 10 | — | 10 | — | ns | |
| CE1# High to WE# Invalid Time for Standby Entry | $t_{CHWX}$ | 10 | — | 10 | — | 10 | — | ns | 1 |
| CE2 Low Hold Time after Power-up | $t_{C2LH}$ | N/A | | 50 | — | 50 | — | µs | |
| CE1# High Hold Time following CE2 High after Power-up | $t_{CHH}$ | 300 | — | 300 | — | 300 | — | µs | |
| Input Transition Time | $t_T$ | 1 | 25 | 1 | 25 | 1 | 25 | ns | 2 |

***Notes:***

1. *Some data might be written into any address location if $t_{CHWX}$(min) is not satisfied.*
2. *The Input Transition Time ($t_T$) at AC testing is 5ns as shown in below. If actual tT is longer than 5ns, it may violate AC specification of some timing parameters.*

# AC Characteristics

## AC Test Conditions

| Symbol | Description | Test Setup | Value | Unit | Note |
|---|---|---|---|---|---|
| $V_{IH}$ | Input High Level | | $V_{DD}$ * 0.8 | V | |
| $V_{IL}$ | Input Low Level | | $V_{DD}$ * 0.2 | V | |
| $V_{REF}$ | Input Timing Measurement Level | | $V_{DD}$ * 0.5 | V | |
| $t_T$ | Input Transition Time | Between $V_{IL}$ and $V_{IH}$ | 5 | ns | |

## AC Measurement Output Load Circuit

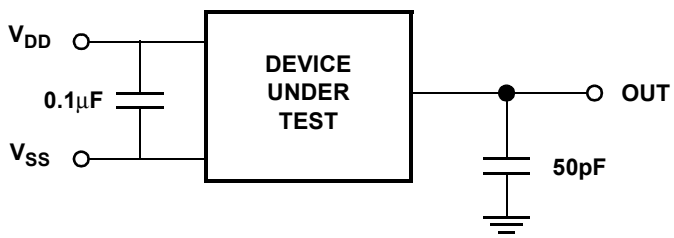



**Figure 32. AC Output Load Circuit**

# Timing Diagrams

## Read Timings

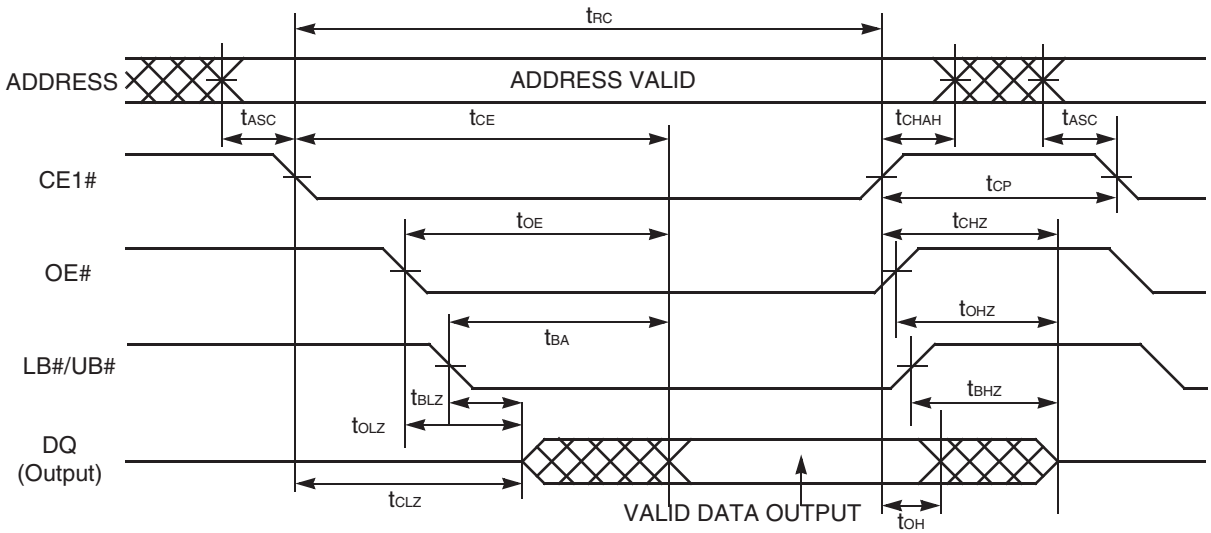



**Figure 33. Read Timing #I (Baisc Timing)**

***Note:*** *This timing diagram assumes CE2=H and WE#=H.*

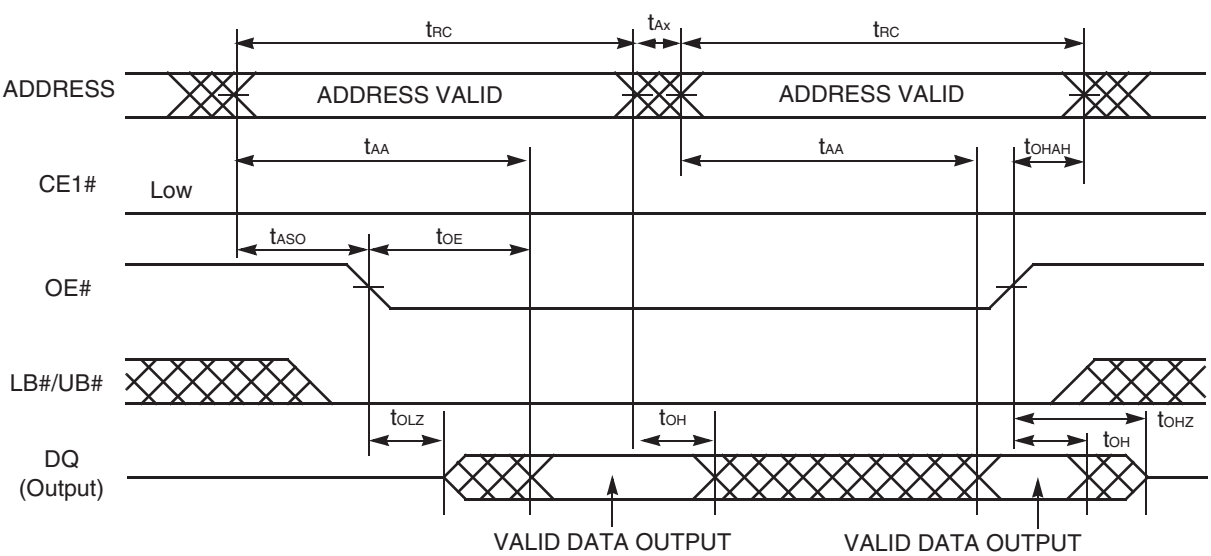



**Figure 34. Read Timing #2 (OE# Address Access**

***Note:*** *This timing digaram assumes CE2=H and WE#=H.*

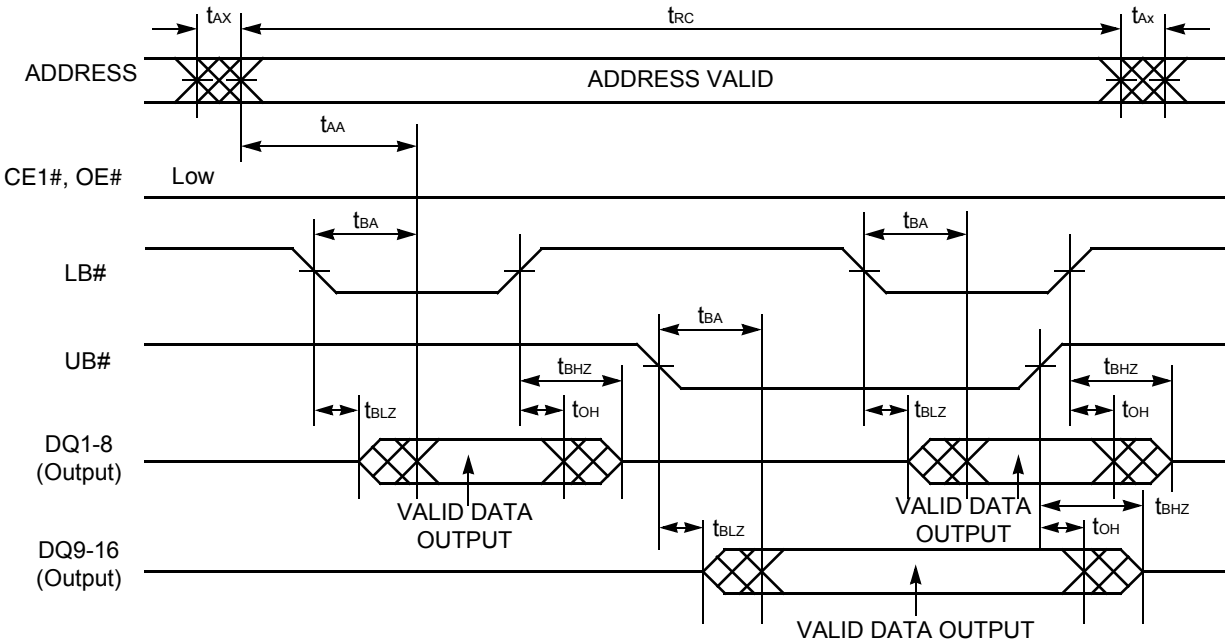



**Figure 35. Read Timing #3 (LB#/UB# Byte Access)**

***Note:*** *This timing diagram assumes CE2=H and WE#=H.*

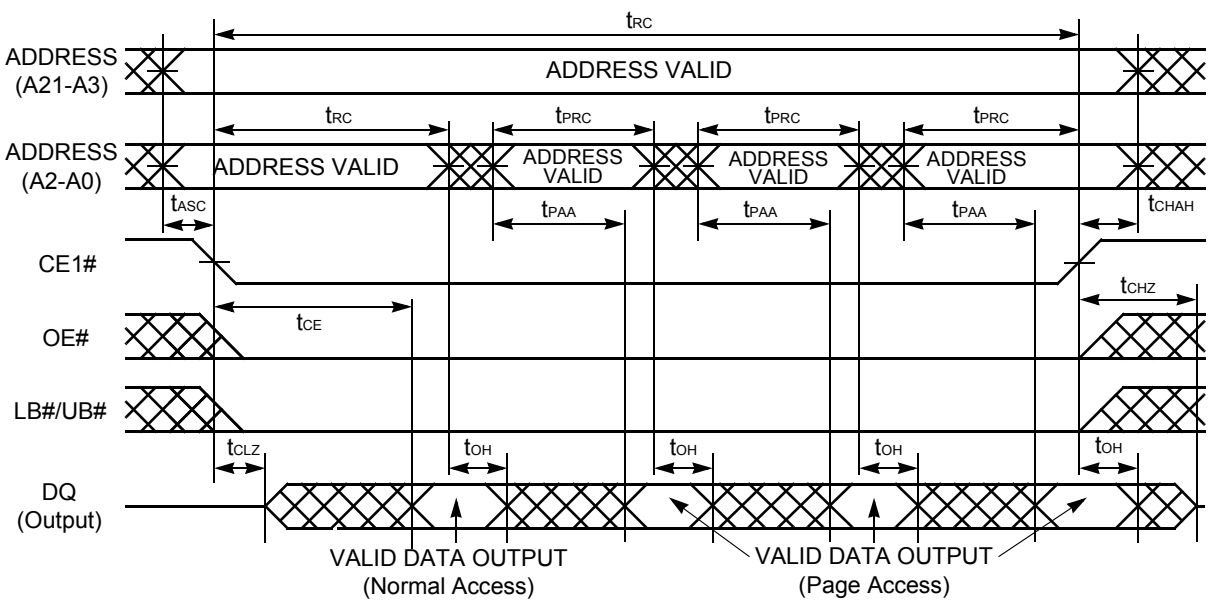



**Figure 36. Read Timing #4 (Page Address Access after CEI# Control Access for 32M and 64M Only)**

***Note:*** *This timing diagram assumes CE2=H and WE#=H.*

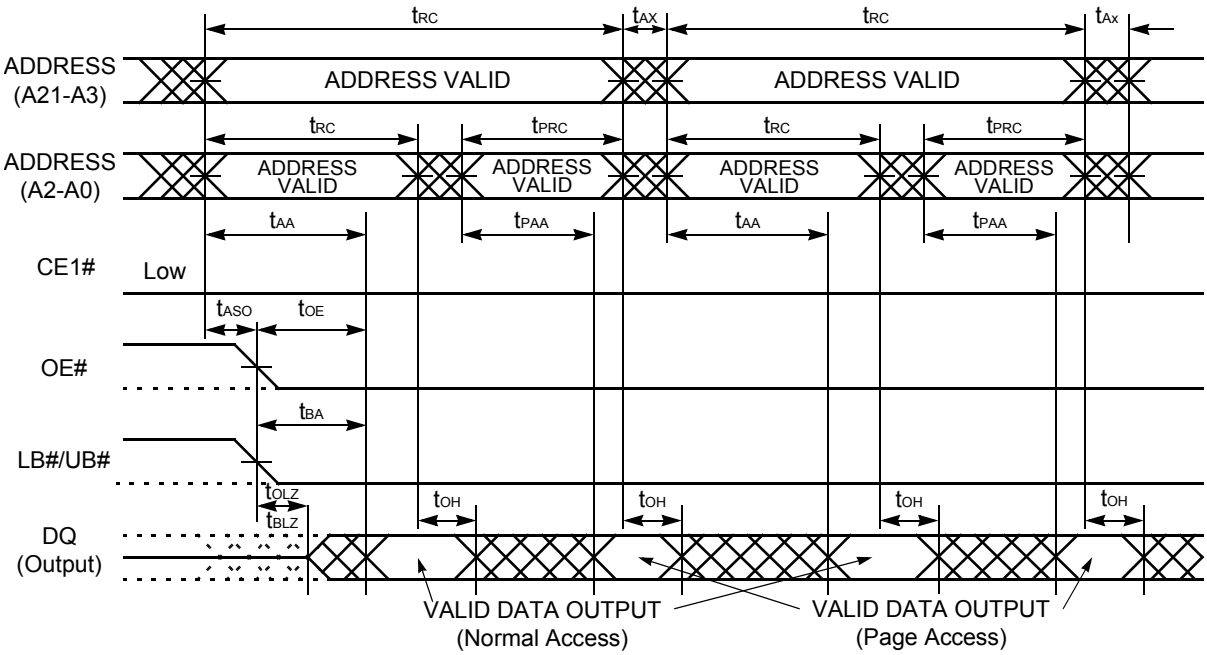



**Figure 37. Read Timing #5 (Random and Page Address Access for 32M and 64M Only)**

***Notes:***

1. *This timing diagram assumes CE2=H and WE#=H.*
2. *Either or both LB# and UB# must be Low when both CE1# and OE# are Low.*

## Write Timings

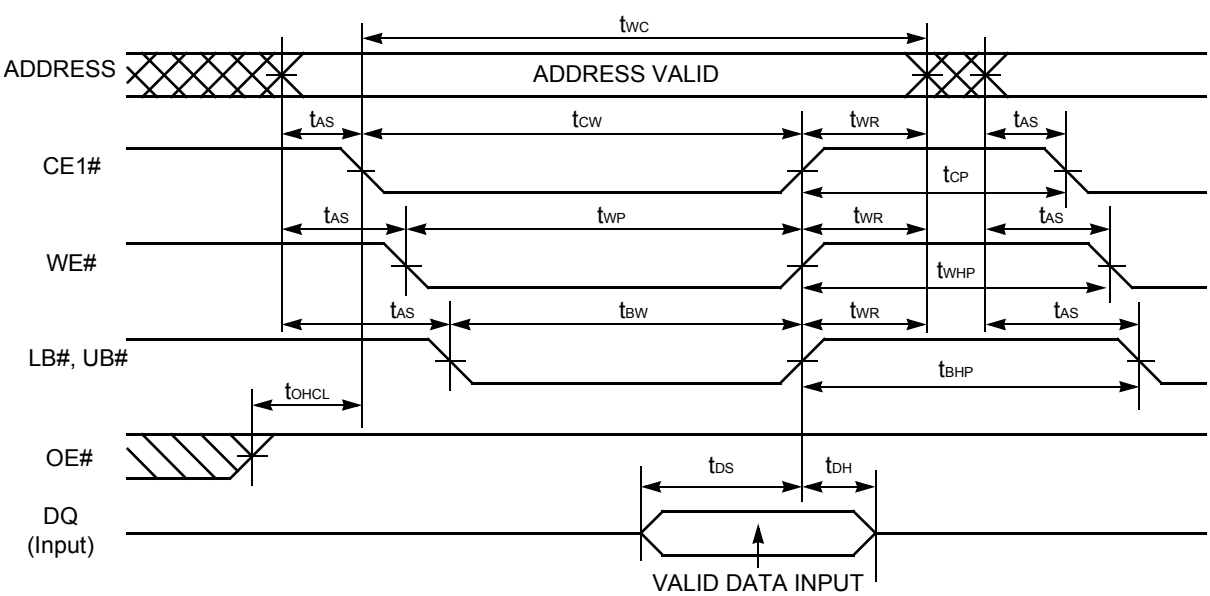



**Figure 38. Write Timing #I (Basic Timing)**

***Note:*** *This timing diagram assumes CE2=H.*

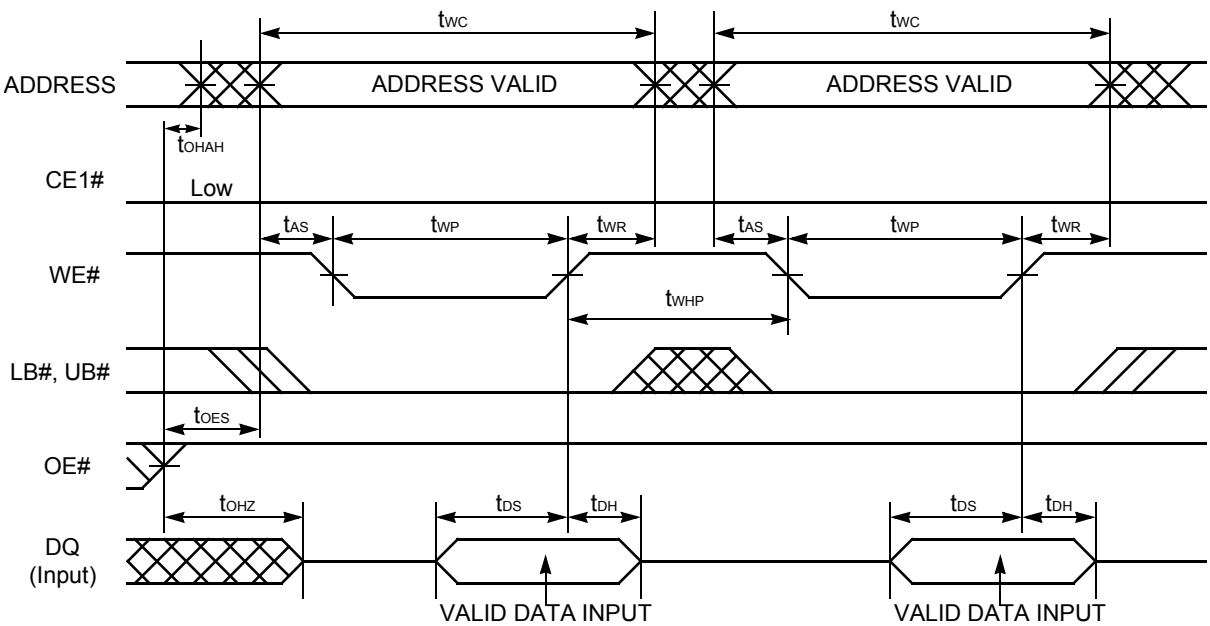



**Figure 39. Write Timing #2 (WE# Control)**

***Note:*** *This timing diagram assumes CE2=H.*

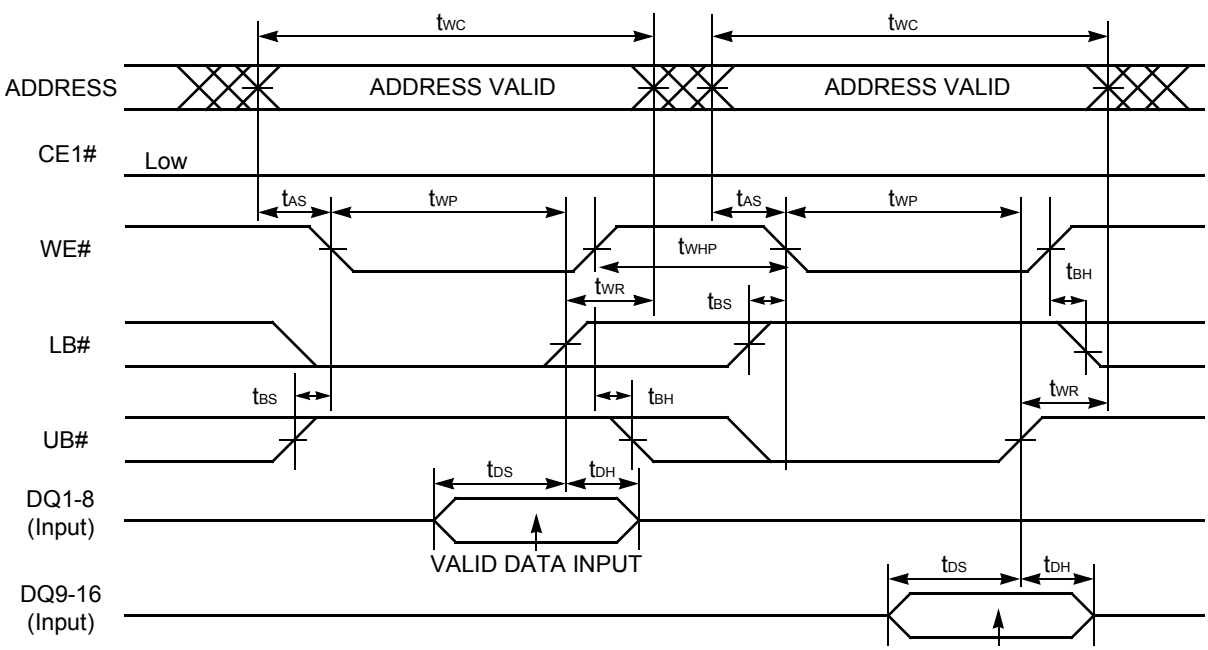



**Figure 40. Write Timing #3-1 (WE#/LB#/UB# Byte Write Control)**

***Note:*** *This timing diagram assumes CE2=H and OE#=H.*

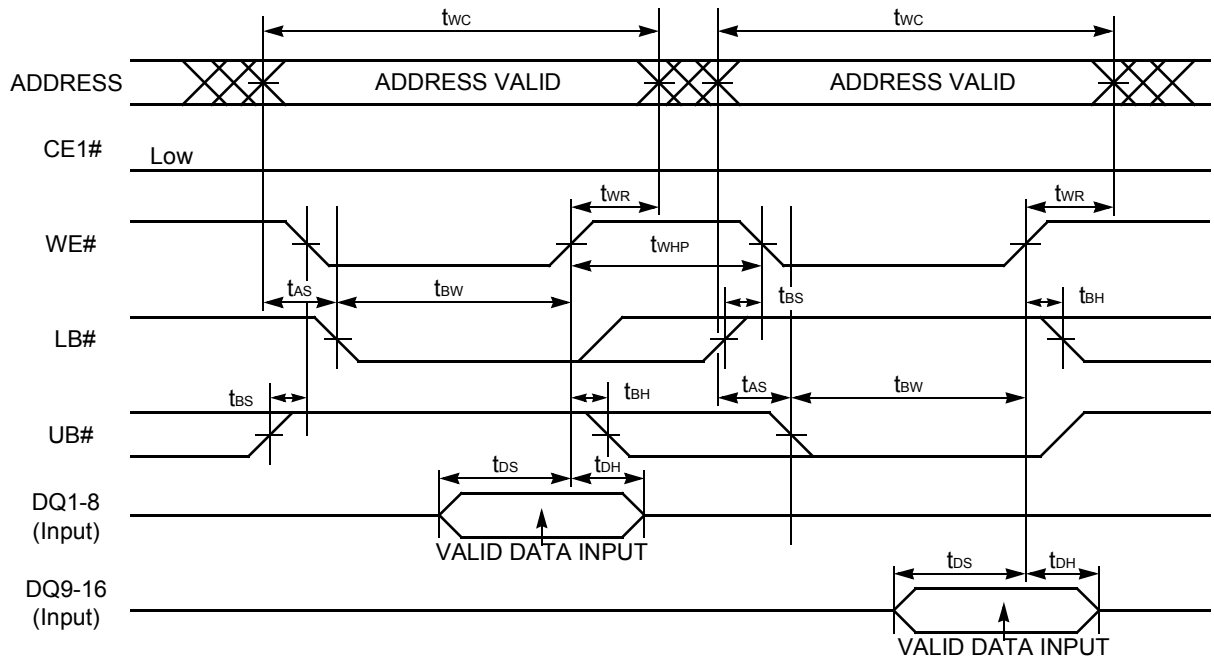



**Figure 41. Write Timing #3-2 (WE#/LB#/UB# Byte Write Control)**

***Note:*** *This timing diagram assumes CE2=H and OE#=H.*

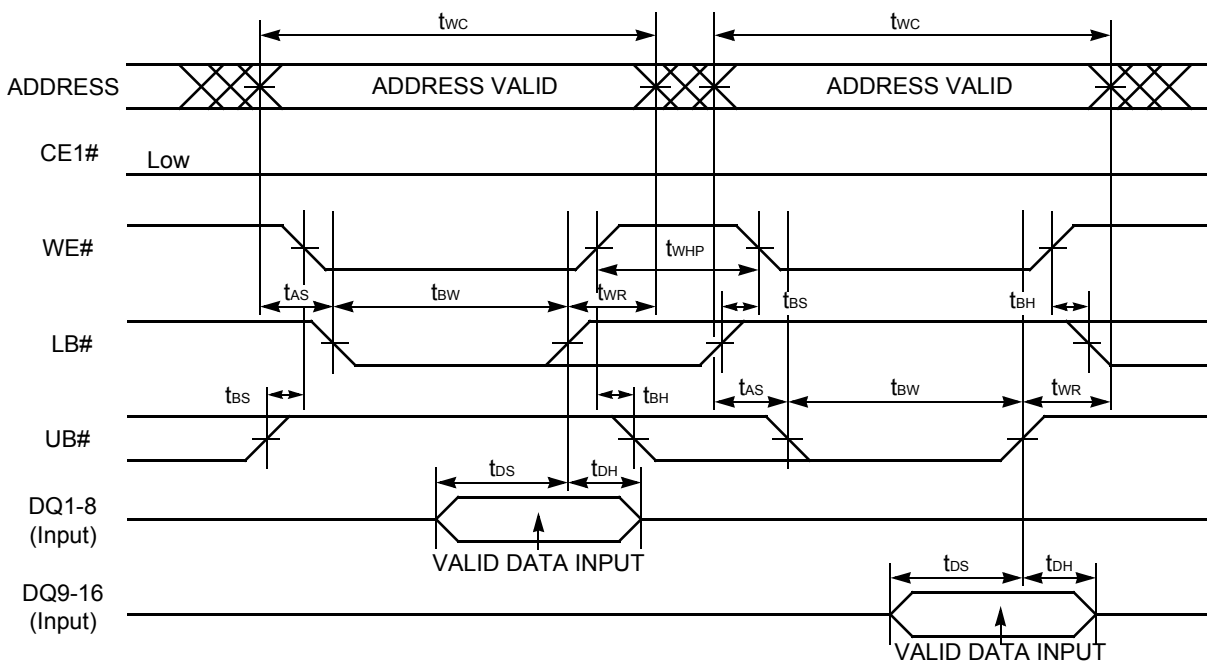



**Figure 42. Write Timing #3-3 (WE#/LB#/UB# Byte Write Control)**

***Note:*** *This timing diagram assumes CE2=H and OE#=H.*

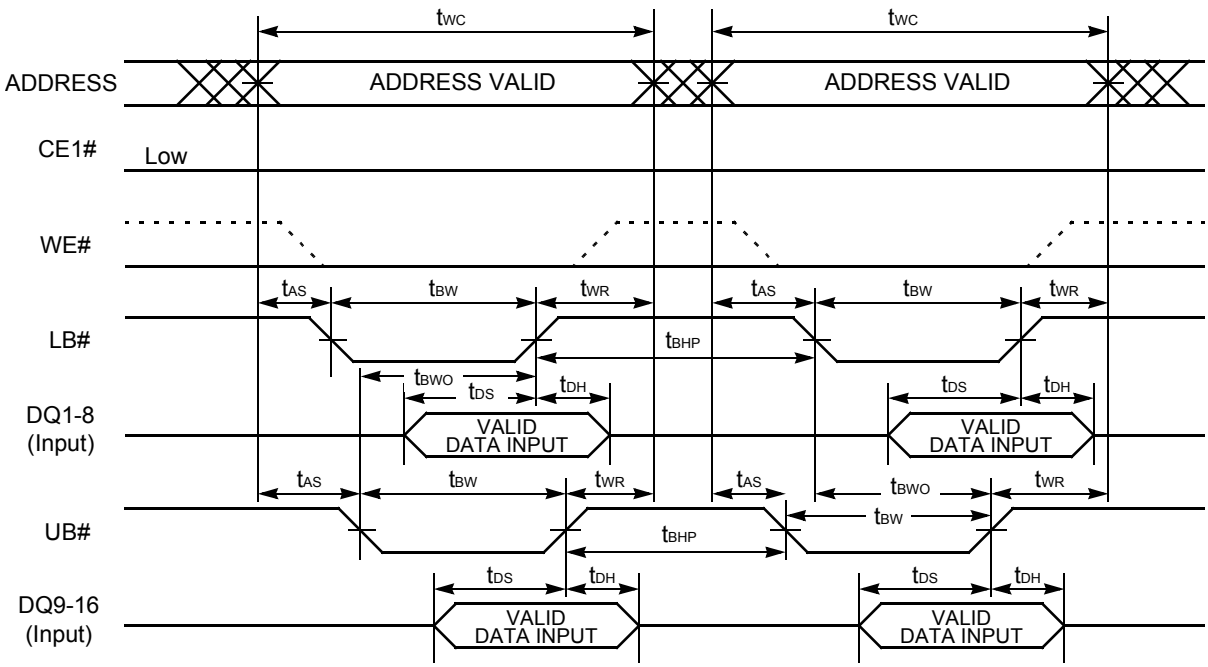



**Figure 43. Write Timing #3-4 (WE#/LB#/UB# Byte Write Control)**

***Note:*** *This timing diagram assumes CE2=H and OE#=H.*

## Read/Write Timings

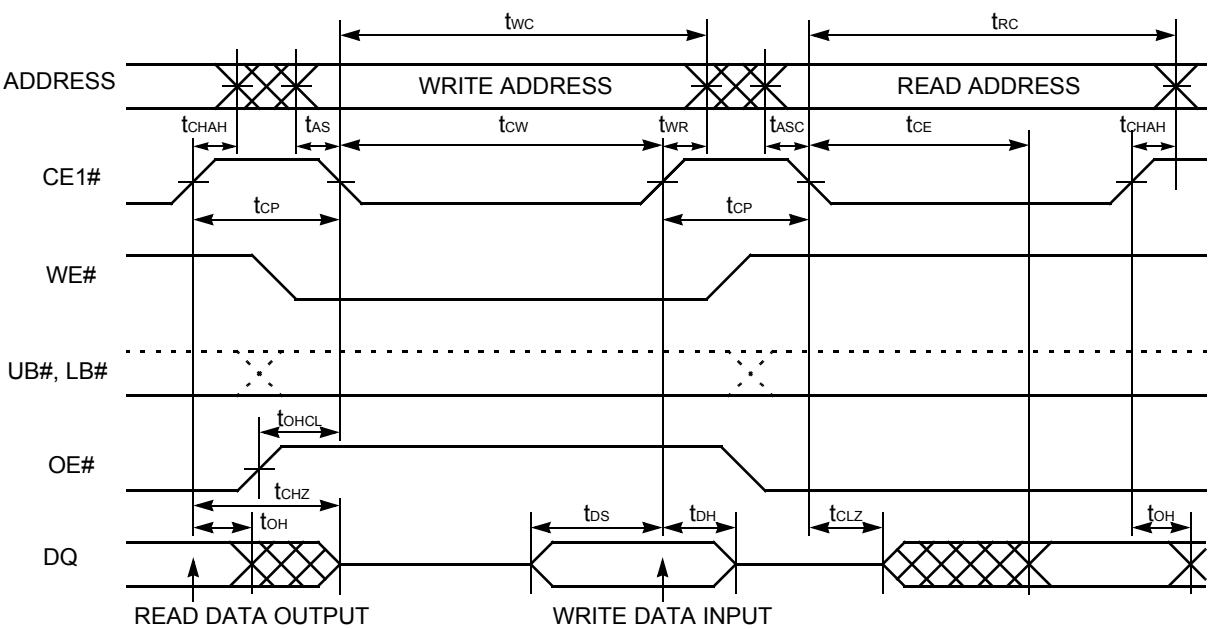



**Figure 44. Read/Write Timing #I-I (CEI# Control)**

***Notes:***

1. *This timing diagram assumes CE2=H.*
2. *Write address is valid from either CE1# or WE# of last falling edge.*

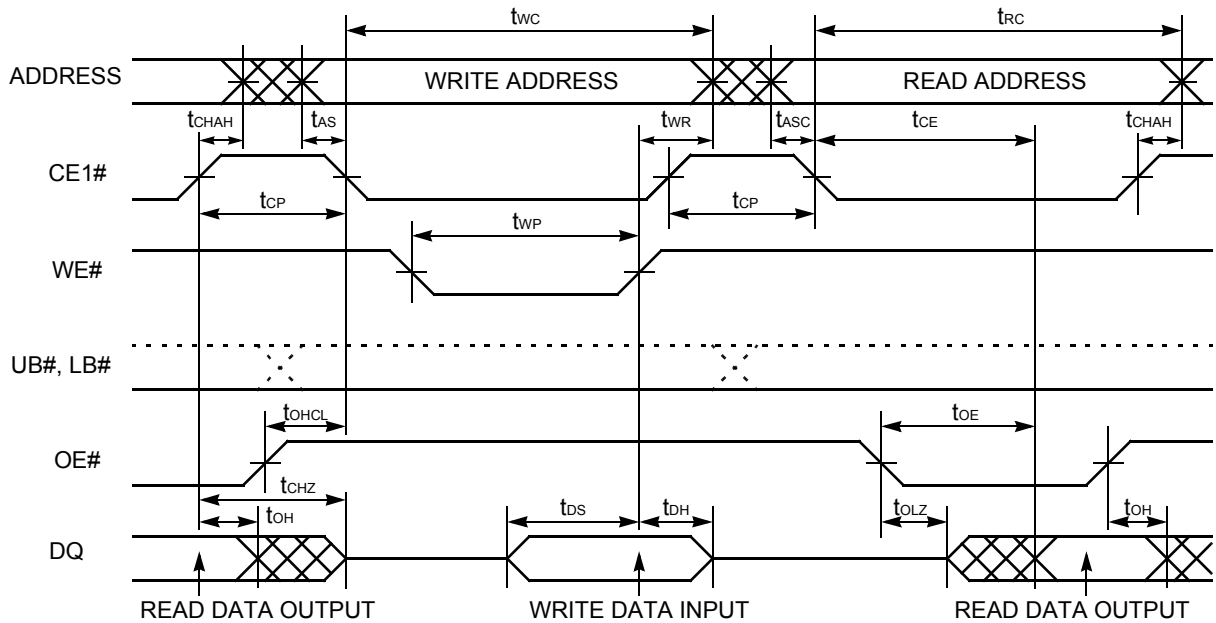



**Figure 45. Read / Write Timing #I-2 (CEI#/WE#/OE# Control)**

***Notes:***

1. *This timing diagram assumes CE2=H.*
2. *OE# can be fixed Low during write operation if it is CE1# controlled write at Read-Write-Read sequence.*

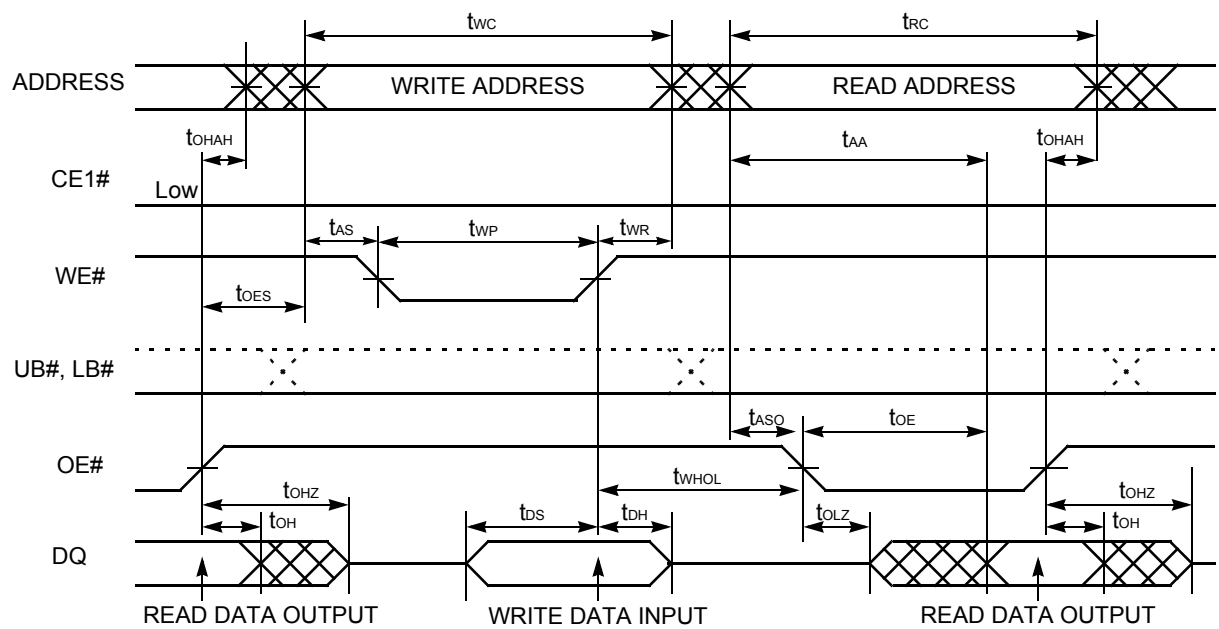



**Figure 46. Read / Write Timing #2 (OE#, WE# Control)**

***Notes:***

1. *This timing diagram assumes CE2=H.*
2. *CE1# can be tied to Low for WE# and OE# controlled operation.*

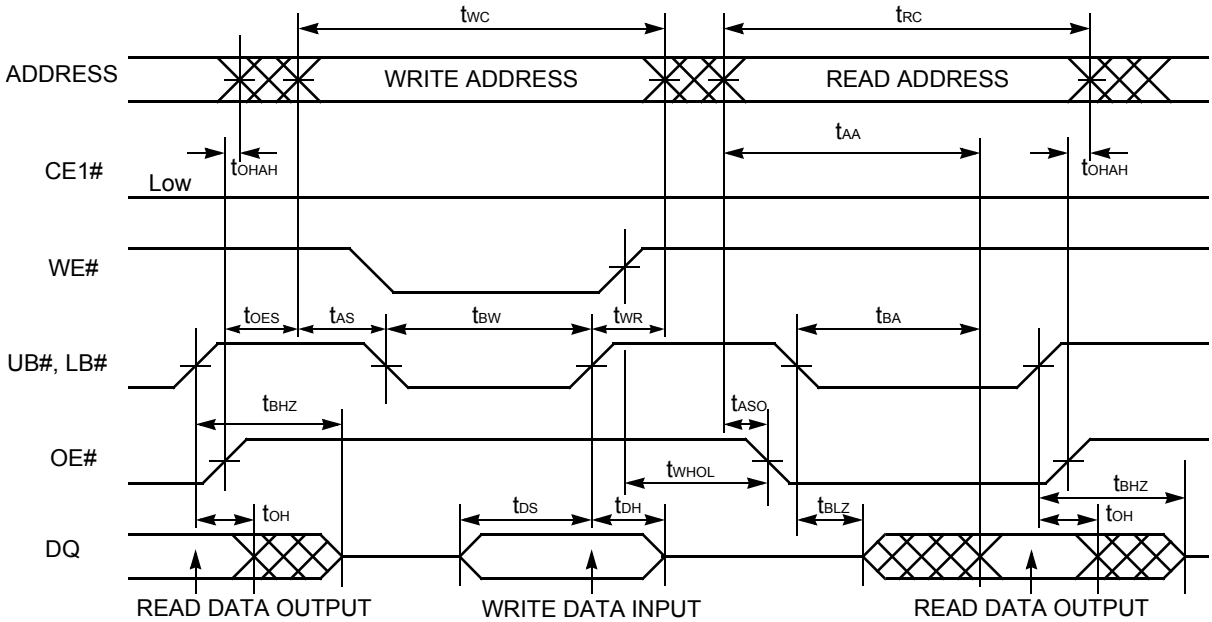



**Figure 47. Read / Write Timing #3 (OE#, WE#, LB#, UB# Control)**

***Notes:***

1. *This timing diagram assumes CE2=H.*
2. *CE1# can be tied to Low for WE# and OE# controlled operation.*

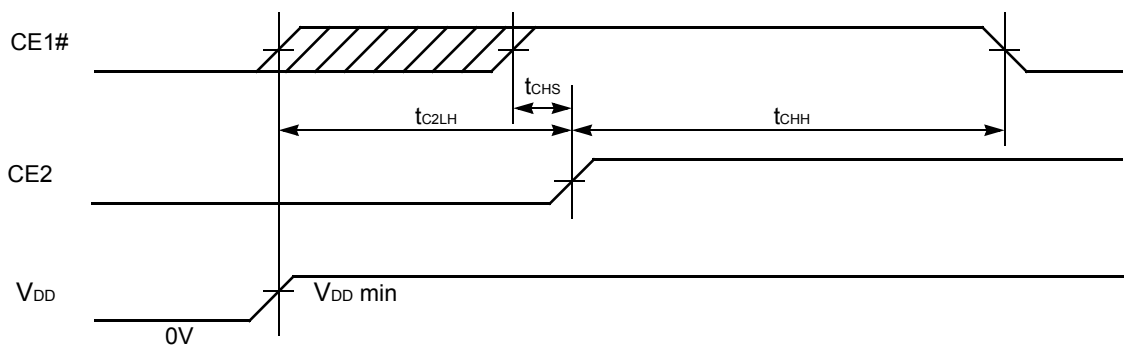



**Figure 48. Power-up Timing #I**

***Note:*** *The $t_{C2LH}$ specifies after $V_{DD}$ reaches specified minimum level.*

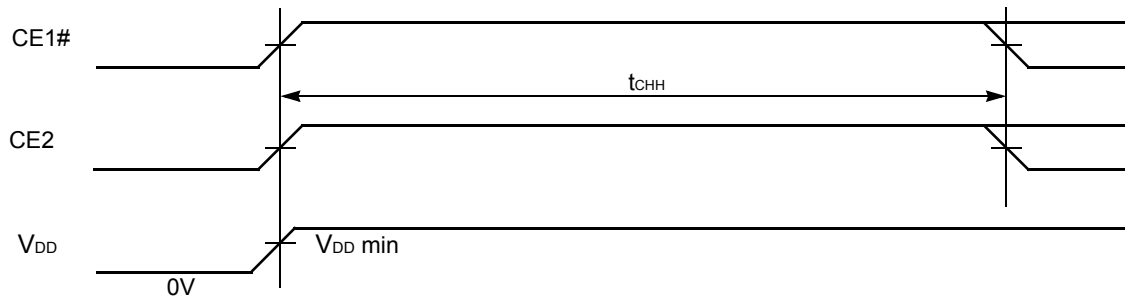



**Figure 49. Power-up Timing #2**

***Note:*** *The $t_{CHH}$ specifies after $V_{DD}$ reaches specified minimum level and applicable to both CE1# and CE2.*

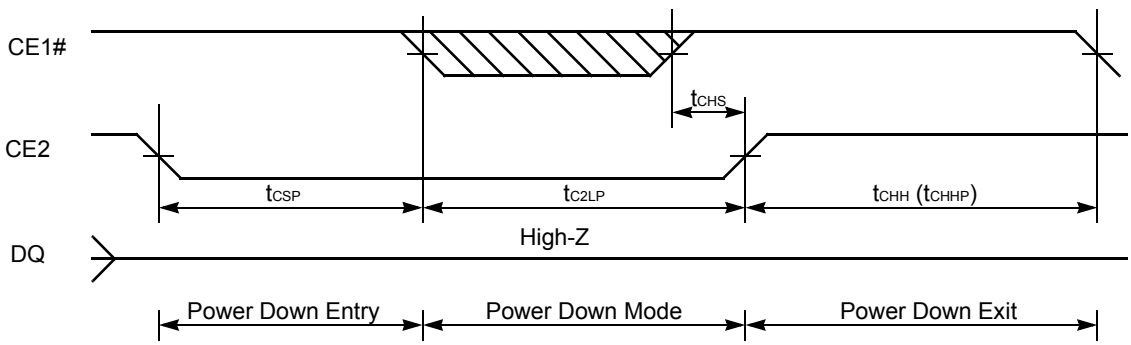



**Figure 50. Power Down Entry and Exit Timing**

***Note:*** *This Power Down mode can be also used as a reset timing if POWER-UP timing above could not be satisfied and Power-Down program was not performed prior to this reset.*

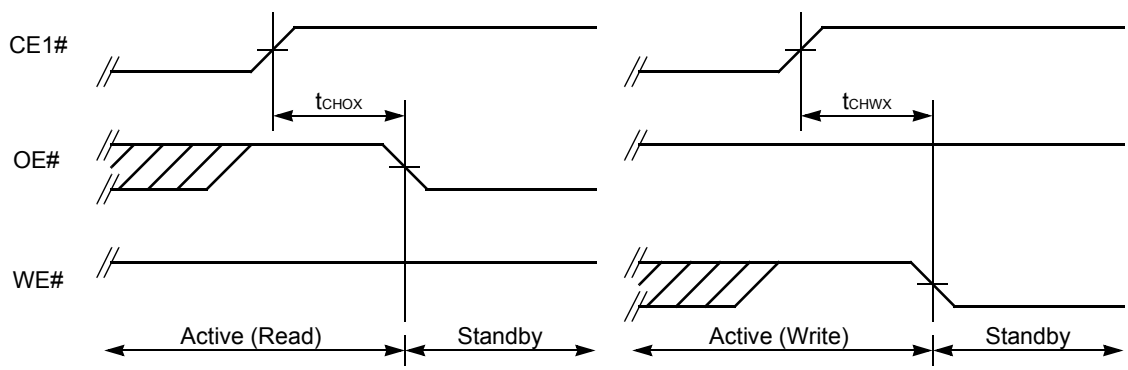



**Figure 51. Standby Entry Timing after Read or Write**

***Note:*** *Both $t_{CHOX}$ and $t_{CHWX}$ define the earliest entry timing for Standby mode. If either of timing is not satisfied, it takes $t_{RC}$ (min) period for Standby mode from CE1# Low to High transition.*

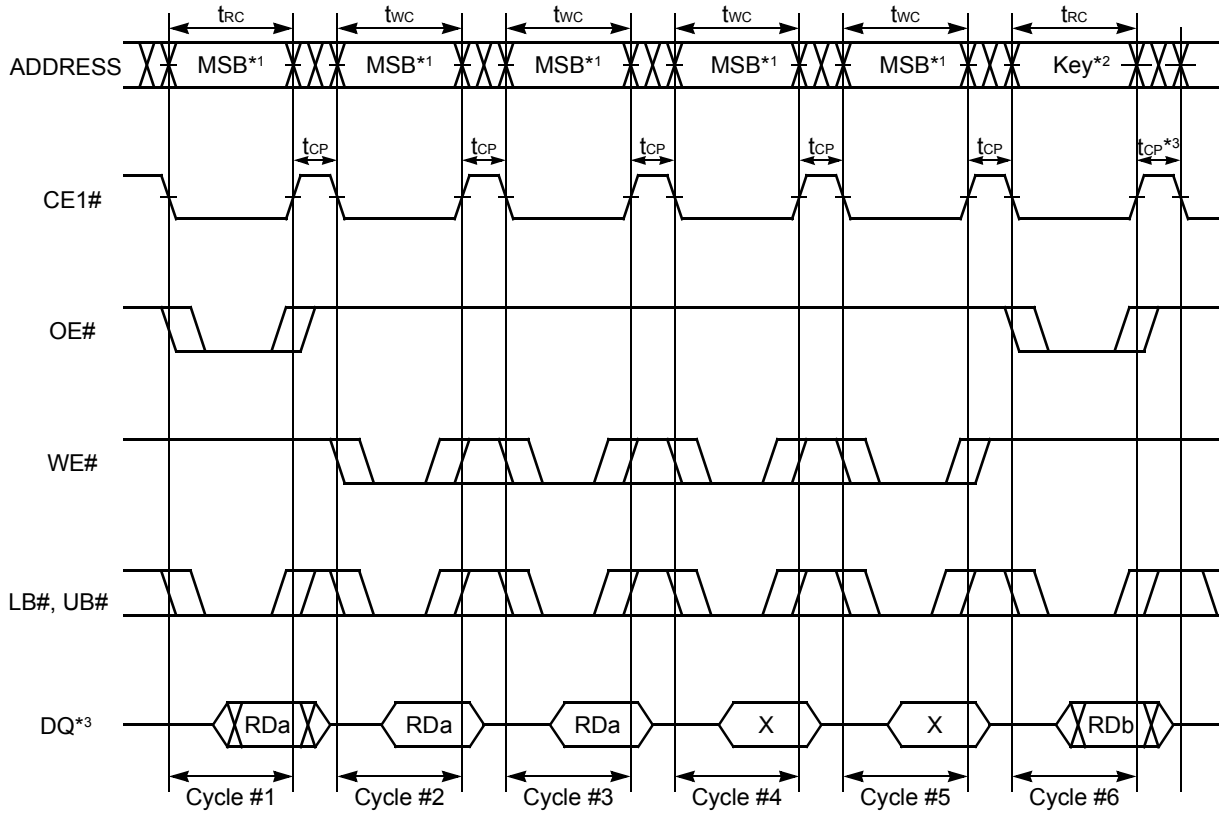



**Figure 52. Power Down Program Timing (for 32M/64M Only)**

***Notes:***

1. *The all address inputs must be High from Cycle #1 to #5.*
2. *The address key must confirm the format specified in page 129. If not, the operation and data are not guaranteed.*
3. *After $t_{CP}$ following Cycle #6, the Power Down Program is completed and returned to the normal operation.*

# Revision Summary

## Revision A (August 24, 2004)

Initial release.

## Revision AI (December 7, 2004)

### Connection Diagrams.

Added 64-ball pinout.

### Ordering Information

Updated the OPN table.

### Valid Combinations tables

Updated all tables.